A Fully Integrated Fractional-N Frequency Synthesizer for Wireless Communications

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A Fully Integrated Fractional-N Frequency Synthesizer for Wireless Communications

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This dissertation is dedicated to

my parents in heaven,

my wife, Youngsahn and my new born son, Ryan Chanki

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always be in my heart and I will teach my son, Ryan Chanki, as they taught me through my life.

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Summary

A fully integrated, fast-locking fractional-N frequency synthesizer is proposed and demonstrated in this work. In this design, to eliminate the need for large, inaccurate capacitors and resistors in a loop filter, an analog continuous-time loop filter whose performance is sensitive to process and temperature variations and aging has been replaced with a programmable digital Finite Impulse Response (FIR) filter. In addition, using the adaptive loop gain control proportional to the frequency difference, the frequency-locking time has been reduced. Also, the phase noise and spurs have been reduced by a Multi-stAge noise SHaping (MASH) controlled Fractional Frequency Detector (FFD) that generates a digital output corresponding directly to the frequency difference. The proposed frequency synthesizer provides many benefits in terms of high integration ability, technological robustness, fast locking time, low noise level, and multimode flexibility.

To prove performance of the proposed frequency synthesizer, the frequency synthesizer's analysis, design, and simulation have been carried out at both the system and the circuit levels. Then, the performance was also verified after fabrication and packaging.

Chapter 1

Introduction

In wireless communication systems, a low manufacturing cost and low power consumption are critical requirements due to highly competitive market environment and limitation in battery life [1]. In the early 80's, circuits with a working frequency over a GHz were implemented using Gallium Arsenide (GaAs) technology. Therefore, GaAs was the main substrate used in circuit design for high frequency blocks to transmit signals in mobile phones. However, since silicon wafers cost much less than GaAs during the 80's, GaAs used in high frequency front-end blocks were often replaced by Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS) or Complementary Metal-Oxide Semiconductor (CMOS). Nowadays, the bipolar transistors' unity-gain bandwidth, f_T, is around 70 GHz, while the unit-gain bandwidth of the Silicon Germanium (SiGe) bipolar transistors is higher than that of classical GaAs Field-Effect Transistors (FETs) and is over 100 GHz. Even CMOS that was not considered an option for high-frequency blocks improved its unity-gain bandwidth to 100 GHz by using device scaling, new materials such as copper for interconnection, and additional metal layers. So, a CMOS technology that is compatible with the digital back-end CMOS is becoming an attractive, cost-effective solution for integrating Radio Frequency (RF) front-ends, with a final goal being the full RF System-on-Chip (SoC) [4].

Market competitions take place both at the technology level to optimize cost and power consumption of mobile communication systems and at the system design level to

implement flexibility into wireless communication systems. While the wireless communication system standards during the 80's varied greatly, a few standards such as the Groupe Special Mobile (GSM) became predominant worldwide while others like the Personal Handy-phone System (PHS) in Japan vanished. Lately, the wireless digital communication systems are categorized into the following groups of standards: GSM-900, Digital Communication System 1800 (DCS-1800), PCS-1900, General-Packet-Radio Service (GPRS), Enhanced Data rate for GSM Evolution (EDGE), Code-Division Multiple Access (CDMA), D-Advanced Mobile Phone Service (D-AMPS), and PDS. However, an increased demand for high-quality, high-performance, multi-user wireless communication systems leads the way toward third generation (3G) communication systems that have capabilities to support high-speed data communication, mobile internet, e-commerce, and video-on-demand such as CDMAOne/CDMA2000, GSM/W-CDMA, Time Division CDMA (TD-CDMA), and Universal Mobile Telecommunications System (UMTS). At the same time, the demand for Wireless Local Area Network (WLAN) systems has steadily increased. The standards for spread spectrum WLAN systems in the 2.4 GHz Industrial, Scientific, and Medical (ISM) include IEEE 802.11, Bluetooth, and HomeRF. These standards have 1 MB/sec data rate and 50 meter cover range as shown in Table 1 [22]. But, general wireless LANs need to support data rates in excess of 10 Mb/sec to replace wired LANs. A several standards have a data rate over 10 Mb/sec such as IEEE 802.11a, IEEE 802.11b, and HIPERLAN but none of these existing standards in WLAN has received a universal acceptance. Therefore, new standards are currently under development to achieve an improved service quality, a lower system cost, and higher data rates [4].

Table 1. Standards of wireless communication systems

Standard	Frequency Range (MHz)	Channel Spacing	Number of Channels	Switching Time	Remarks
GSM	Rx: 935 – 960 Tx: 890 – 915	200 KHz	124	800 us	
DCS 1800	Rx: 1805 – 1880 Tx: 1710 – 1785	200 KHz	374	800 us	
PCS 1900	Rx: 1930 – 1990 Tx: 1710 – 1785	200 KHz	-	800 us	
DECT	1880 – 1900	1.728 MHz	10	450 us	
AMPS	Rx: 869 – 894 Tx: 824 - 849	30 KHz	832	slow	
CDMA	Rx: 869 – 894 Tx: 824 – 849	1.25 MHz	20	-	
PHS 1900	Rx: 1895 – 1918	300 KHz	300	1.5 ms	
IS 54	Rx: 869 – 894 Tx: 824 – 849	30 KHz	832	slow	

	IEEE 802.11	HomeRF	Bluetooth
Frequency band	2.4 GHz ISM	2.4 GHz ISM	2.4 GHz ISM
Modulation	DSSS	FHSS, 50 hops/s	FHSS, 1000 hops/s
Data rate	1 Mb/s	1 Mb/s	1 Mb/s
Power	20 dBm	20 dBm	0 dBm, 20 dBm
Range	50 m	50 m	50 m
Topology	access point	access point	Ad hoc

A transceiver is a building block that interfaces between the user and the transmission medium and consists of three components: the front-end block for

converting the RF signal to a base-band signal, the back-end block for modulating and demodulating the signal between analog and digital domains, and the user-end interface between the user input and its digital data representation. Of these three components, the front-end block can be divided into two parts: a receiver and a transmitter [4].

There are two well-known receiver types: the homodyne or zero-Intermediate Frequency (IF) and the heterodyne. The heterodyne receiver architecture is shown in Figure 1. In a heterodyne wireless receiver, the weak radio-frequency signal picked up by the antenna is filtered by a RF filter and amplified by a Low Noise Amplifier (LNA). The LNA provides image rejection, noise reduction, and prevention of feed-through signal from the Local Oscillator (LO) to the antenna. Next, the amplified RF signal is fed to the first mixer and combined with a locally synthesized signal $f_{LO1}(= f_c - f_{IF})$ to generate a new frequency signal. Since the output frequency of the down-convert mixer is the absolute value of the difference between the two input signals, both the desired signal at f_C and the image signal at $(f_C - 2 \cdot f_{IF})$ are mixed down to IF [22].

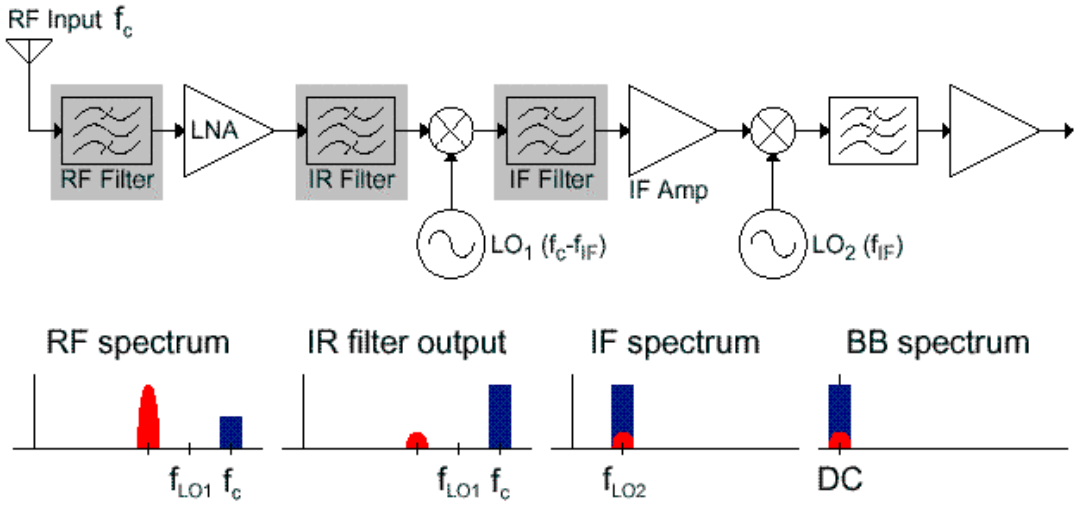


Figure 1. Heterodyne receiver

Therefore, the RF signal must be filtered by the Image Rejection (IR) filter that is usually implemented using the Surface-Acoustic Wave (SAW) filter in order to remove the image signal at (f_C - $2 \cdot f_{IF}$) before the image signal is down-converted. As the mixer performs the frequency subtraction, the resultant signal at the IF will pass through the channel selection filter. Thus, only the desired channel signal remains and is sampled by the Analog-to-Digital Converter (ADC) [2].

The following details how the heterodyne receiver works after the filtering by the IR filter under the GSM standard. First, the mixer mixes down the desired channel within the receiver frequency band to exactly 70 MHz where the IF channel selection filter is centered to remove all unwanted channels. Therefore, when the receiver frequency band is from 935 MHz to 960 MHz and the IF is 70 MHz, the frequency synthesizer's output frequency should be from 865 MHz to 890 MHz in order to remove all unwanted channels. The frequency resolution of the frequency synthesizer should be 200 KHz because the channel spacing in the receiver band is 200 KHz in the GSM standard. Once the selected channel signal is converted to the IF frequency by first mixer in the heterodyne system, it is fed to the IF amplifier. Then, the amplified IF signal is combined with the fixed local signal, f_{LO2} and is down-converted to a base-band signal by the second mixer. Therefore, a desired channel can be selected from the crowded RF spectrum by varying the frequency of the locally synthesized signal, f_{LO1}. So, a frequency synthesizer used as a local oscillator is a critical building block for wireless communication systems [2,3].

The important system performance specifications for a frequency synthesizer are synthesized output signal's purity, frequency locking time, power dissipation, multi-standard flexibility, and manufacturing cost [2,3].

The purity of the synthesized output signal in terms of phase noise and sideband spurs is imperative in any phase-modulated system. Ideally, this means the output of the frequency synthesizer should be a pure tone. However, the oscillation frequency phase will fluctuate due to either the thermal noise generated by resistors and transistors in the oscillator or the noise at the frequency-tuning input of the oscillator. The phase fluctuation then forms a skirt of noise power around the carrier impulse in the frequency domain. As shown in Figure 2, an interference signal near the small desired signal is usually large, so the skirt of phase noise around the LO signal degrades the Signal-to-Noise Ratio (SNR) of the desired signal.

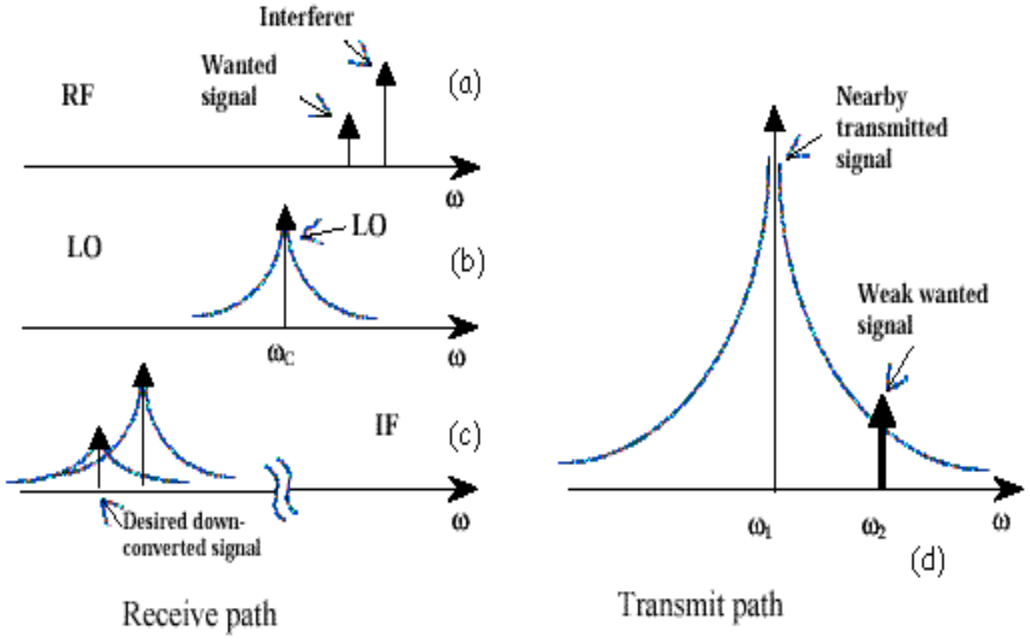


Figure 2. Effect of phase noise on the LO signal

The phase noise is defined as the difference between the carrier power and the total noise power within 1 Hz at a frequency offset, Δf, from the carrier frequency.

In addition to the phase noise caused by the internal thermal noise and the external input noise, the oscillator output can also be modulated by the fixed frequency noise coming from the switching of synthesizer circuits. The input noise will modulate the oscillator output and be up-converted to the carrier. Two tones will then appear at the upper and lower sidebands of the carrier. These two tones are called spurs and are measured by the difference between the carrier powers and the spurs at some frequency offset in the dBc unit. Similar to the case of phase noise, if a large interference signal is present near the desired signal and the local oscillator signal has spurs, then both the desired and the interference signals will be mixed down to intermediate frequency, as shown in Figure 3. Therefore, if the spur in the down-converted interferer is at the same frequency as the desired signal, the SNR of the desired signal is degraded [4].

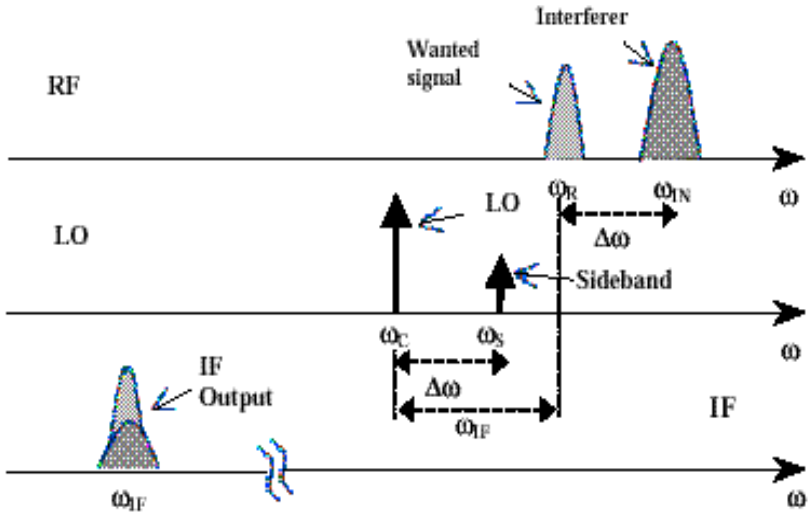


Figure 3. Effect of spurs on the LO signal

One of the most important performance specifications, fast locking time from one frequency to another is necessary to meet time-slot requirements for the time-division multiple-access systems such as GSM, PHS, and Personal Digital Cellular (PDC). For a fast frequency-hopping system, the locking speed requirement is even more stringent [13].

With power management becoming essential for portable devices, a higher switching speed became a solution for reducing power dissipation. For example, a faster frequency synthesizer makes it possible to reduce the on-duty cycle time of a pager receiver, which in turn reduces power dissipation.

Another requirement, low manufacturing cost, can be achieved by a monolithic implementation of required functions. Specifically, low power consumption and a low cost can only be achieved together by using a high degree of integration. Therefore, transceivers are in the process of quickly migrating from a three- or four-chip solution with several external components (such as capacitors, resistors, and Surface-Acoustic Wave (SAW) filters) to a two-chip solution (one for Digital Signal Processing (DSP) and the other for analog and RF signals processing) with some external components.

With all the above requirements, designing a high-performance, highly integrated frequency synthesizer that operates at several GHz is quite a challenge. The phase noise level and the frequency locking time must meet stringent specifications, and the power dissipation and manufacturing costs must be minimized. Specifically, a system must have a flexibility to support multi-band and multi-standard capabilities. An example is a single system that supports both GSM-900 and DCS-1800. Therefore, this thesis addresses some of the requirements and problems in conventional frequency synthesizer architecture. A frequency synthesizer with low phase noise, fast locking speed, low

manufacturing cost for Bluetooth application, and flexibility for easy adaptability to multi-band, multi-standard applications without external components such as capacitors and resistors has been implemented. All components necessary in implementing a frequency synthesizer, such as a Fractional Frequency Detector (FFD), a reference divider, an amplitude detector, a variable gain block, an accumulator, a Finite-Impulse Response (FIR) digital filter, an eight-bit Digital-to-Analog Converter (DAC), a Voltage-Controlled Oscillator (VCO), a prescaler, and a third-order Multi-stAge noise SHaping (MASH) engine for frequency controller have been designed and fabricated with a 0.18 um CMOS technology with five-metal layers.

This thesis is organized into the following chapters. In the second chapter, an overview of the basic architecture including its transient analysis results and system model for achieving high-performance frequency synthesizers are discussed. Chapter two also includes Phase-Locked Loop (PLL) block diagrams and their transfer functions, which provide operating and design optimization concepts of frequency synthesizer. In Chapter 3, the working theory, advantages, and disadvantages of several frequency synthesizers such as table look-up synthesizer, Direct Digital Frequency Synthesizer (DDFS), charge-pump PLL, dual-loop PLL, fractional-N frequency synthesizer, and All-Digital Frequency Synthesizer (ADFS) are discussed. In Chapter 4, the principle and architecture of the proposed frequency synthesizer and its system-level implementations are presented. Then, the circuit-level design techniques for implementing all components necessary in a frequency synthesizer are reviewed, including MASH engine for frequency modulus controller and FIR digital loop filter. In Chapter 5, the measurement set-up, the PCB design method, test instruments, and the measurement results of the frequency

synthesizer will be covered. Finally, conclusions, contributions and future work for this thesis are given in Chapter 6.

Chapter 2

An Overview and Modeling of PLLs

Frequency synthesizers are an essential part of nearly all multi-frequency wireless transceivers. Phase-Locked Loop (PLL) based frequency synthesizers are most frequently used as local oscillators (LOs) in wireless receivers to down-convert the carrier frequency to a lower, intermediate frequency. Sometimes, PLLs are also used to perform frequency or phase modulation and demodulation, clock recovery, jitter suppression in communication, frequency synthesis, skew suppression, edge detection, etc [2]. In this chapter, the operation of a basic PLL and its transfer function model are demonstrated, then different implementation methods for frequency synthesizers including the PLL-based frequency synthesizer are discussed and compared in terms of their phase noise, frequency locking speed, and manufacturing cost. Some of the implementation methods discussed in the next few sections are currently in wide use.

2.1 Introduction

A majority of frequency synthesizers use a PLL [5]. A PLL is a feedback system that operates on the excess phase of periodic signals. As shown in Figure 4, a simple PLL consists of a Phase Detector (PD), a Low-Pass Filter (LPF), and a Voltage-Controlled Oscillator (VCO).

In the PLL architecture, the PD serves as an error amplifier in the feedback loop. Using this error amplification, the phase difference, $\Delta\phi$, between the input signal, x(t),

and the output signal, y(t), can be minimized. The PLL loop is considered to be in a lock status when the phase difference is constant with time as a result of equal input and output frequencies. In the locked condition, all signals in the loop reaches a steady state and the PLL operates as follows: the phase detector produces an output whose DC value is proportional to the phase difference between input and output signals. Then, the low-pass filter suppresses high-frequency components in the PD output and allows the DC value to control the VCO frequency. Finally, the VCO oscillates at a frequency equal to the input frequency and with a phase difference equal to $\Delta\phi$. Thus, the LPF generates the proper control voltage for the VCO [6].

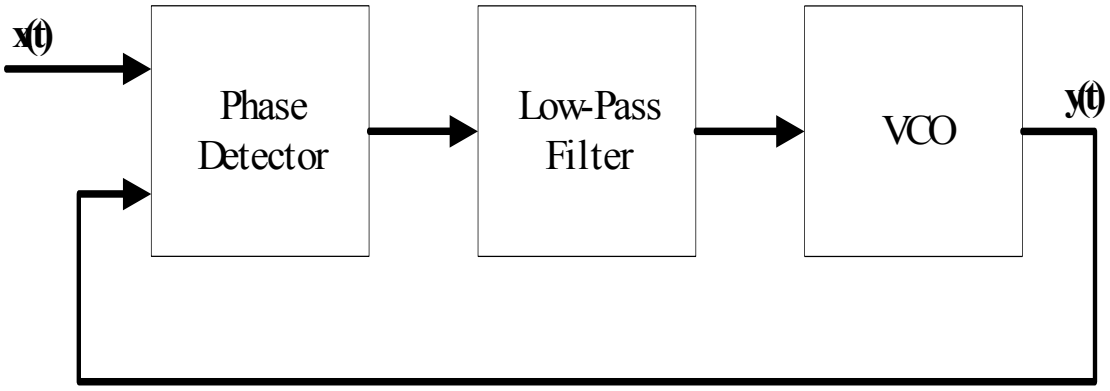


Figure 4. A basic phase-locked loop

Figure 5 shows the signals at various points of a typical PLL that has only a small phase difference between the input and output signals. At first, the PD generates pulses whose widths are equal to the time difference between zero crossings of the input and output. Next, these pulses are low-pass filtered to produce the DC voltage that sustains the VCO oscillation at the required frequency.

In Figure 6, the overall response of the PLL that was in a locked status before ($t = t_0$) but which enforced a small frequency shift at its input ($t = t_0$) is shown. The phase detector generates increasingly wider pulses because the input frequency is temporarily faster than the VCO output frequency. Each of these wider pulses creates an increasingly higher DC voltage at the output of the LPF.

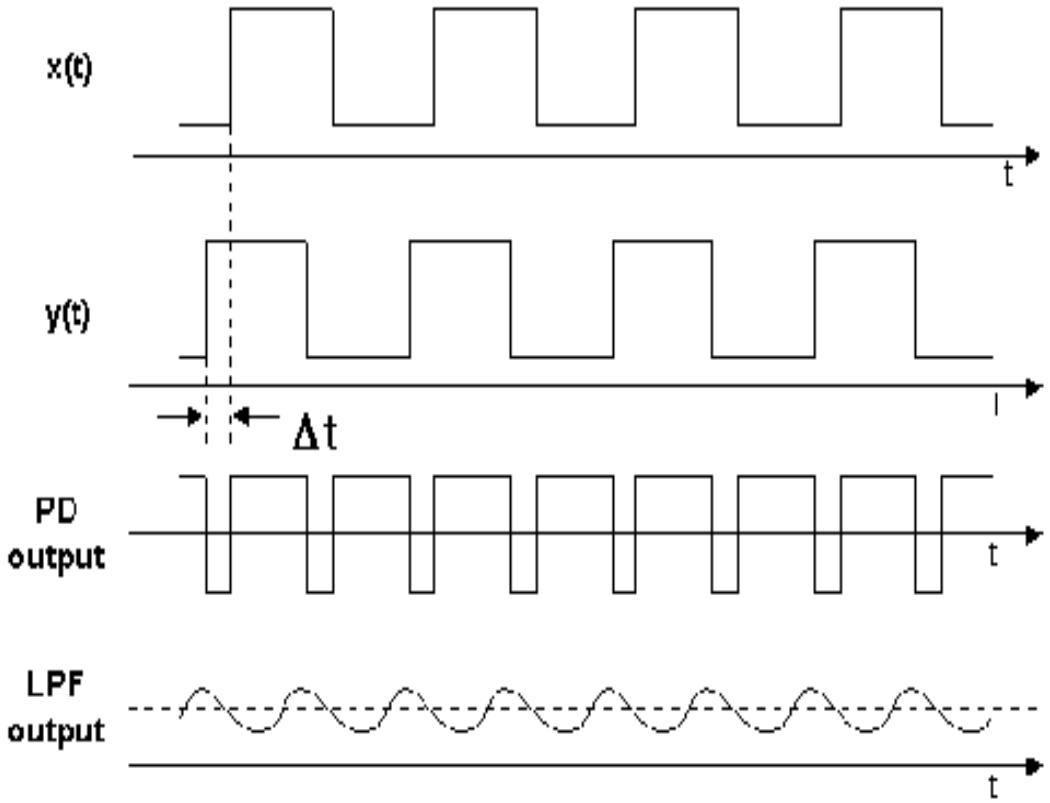


Figure 5. Waveforms in a PLL

Then, the higher DC output voltage of LPF increases the VCO output frequency. As the difference between the input and output frequencies is diminished by the negative feedback function, the width of the phase comparison pulses decreases. Eventually, the DC output voltage of LPF becomes slightly greater than its value before ($t = t_0$) [3].

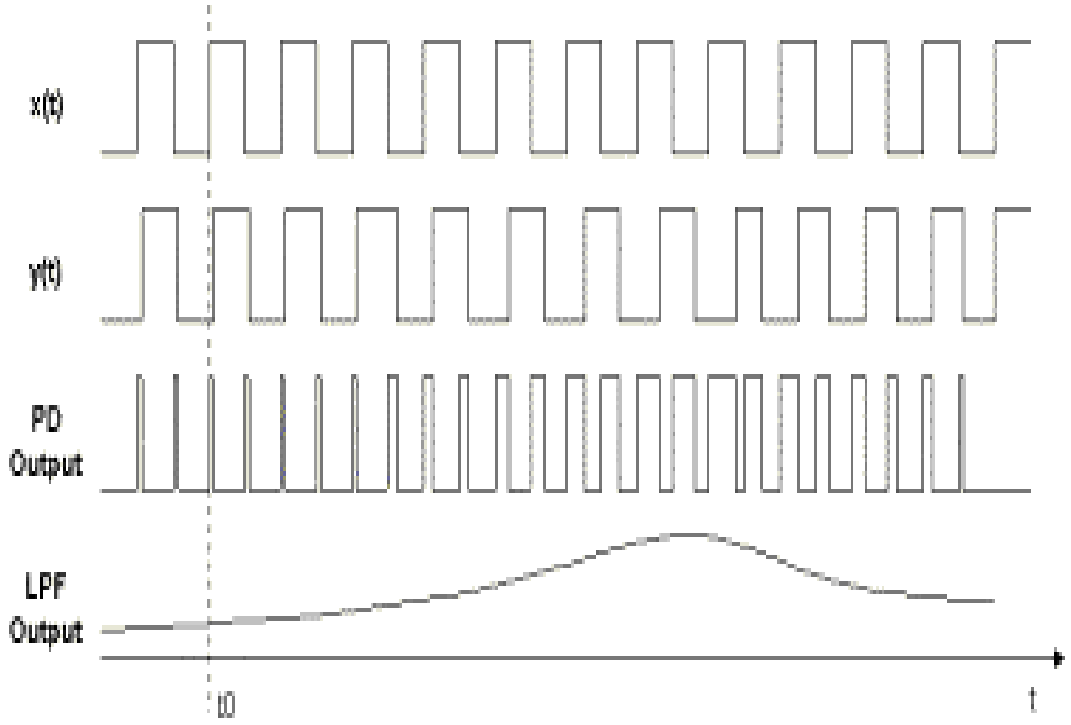


Figure 6. Response of a PLL to a small frequency step

2.2 Modeling and Analysis of PLL

Although a PLL is normally a non-linear device because of phase and frequency detector (PFD), divider, and prescaler, it can be accurately analyzed using a linear device model when the loop is in a locked status.

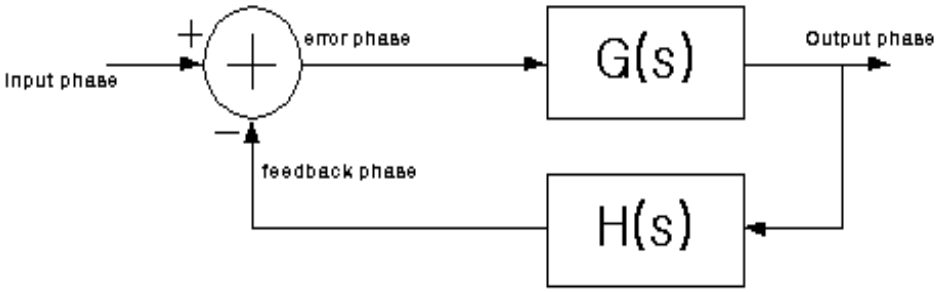


Figure 7. A single loop feedback control system

A basic linear feedback control system is shown in Figure 7. This control system model will be used to derive and analyze the transfer functions of a PLL. In this system model, the closed-loop transfer function is given as a function of feed-forward gain, G(s), and feedback gain, H(s), like G(s) / (1 + G(s) • H(s)), where s is a complex frequency. Another important feature of the system model is the steady-state error transfer function 1 / (1 + G(s) • H(s)) [7], which indicates the remaining error after all transients have died out.

If the system loop bandwidth is less than 20 times the reference input frequency and the system is in a locked status, then the digital PLL which consists of a divider with modulus N, a PFD with gain K_{pd} (V/rad), a LPF with transfer function F(s), and a VCO with gain K_{vco} (rad/sec·V) can also be analyzed using a continuous single-loop feedback control system model. The small-signal block diagram of the simple digital PLL where input signal with a frequency of f_i and a phase θ_i is applied is shown in Figure 8. In this figure, the closed-loop transfer function can be given by

$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{f_o(s)}{f_i(s)} = \frac{G(s)}{1 + G(s) \bullet H(s)} \qquad \text{(eq. 1)}$$

$$\text{where } G(s) = \frac{K_{pd}K_{vco}F(s)}{s} \qquad \text{(eq. 2)}$$

$$\text{and } H(s) = \frac{1}{N} \qquad \text{(eq. 3)}$$

The steady-state error transfer function can also be given by

$$E(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{1}{1 + \frac{K_{pd}\, K_{vco}\, F(s)}{Ns}} \qquad \text{(eq. 4)}$$

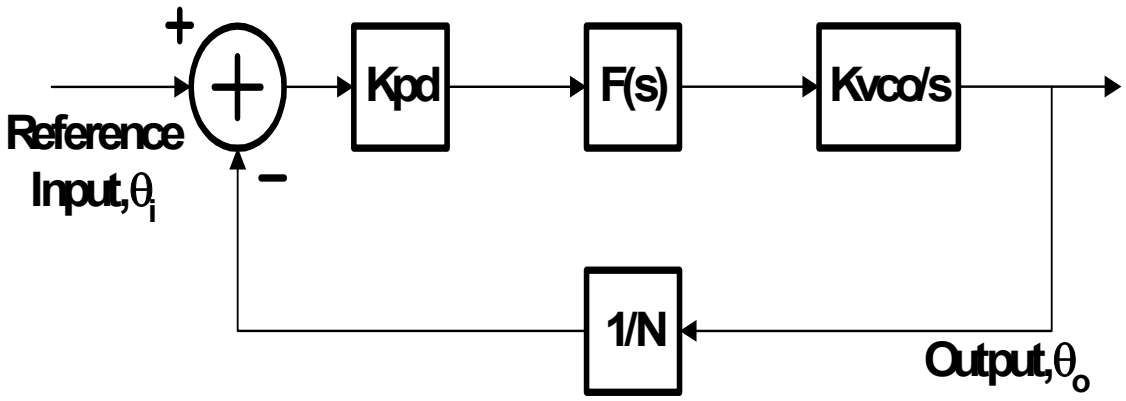


Figure 8. Small signal block diagram of the PLL

As shown in Figure 9, if a simple lag RC filter is used as a loop filter whose transfer function is $F(s) = 1 / (1 + \tau \cdot s)$ where $\tau = R \cdot C$, then the closed-loop transfer function becomes

$$B(s) = \frac{N K_{pd} K_{vco}}{N \tau s^2 + N s + K_{pd} K_{vco}} \qquad \text{(eq. 5)}$$

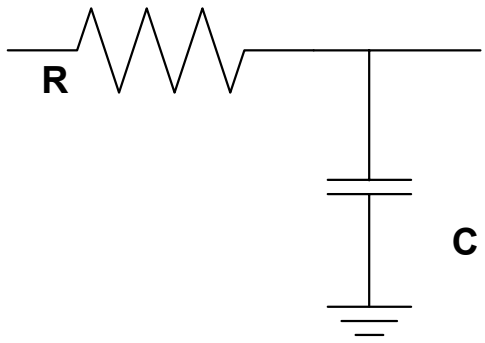


Figure 9. A lag RC filter

The open-loop transfer function of this system has one pole at the origin and the highest degree of this PLL system is two. So, this system is described as a type-one, second-order system. The type-one, second-order system can be mapped to a standard

second-order control system form using standard parameter definitions. After the mapping, the equation (5) becomes

$$B(s) = \frac{N\,\omega_n^2}{s^2 + 2\,\zeta\,\omega_n\,s + \omega_n^2} \qquad \text{(eq. 6)}$$

$$\text{where } \omega_n = \sqrt{\frac{K_{pd}\,K_{vco}}{N\,\tau}} \qquad \text{(eq. 7)}$$

$$\text{and } \zeta = \frac{1}{2}\sqrt{\frac{N}{K_{pd}\,K_{vco}\,\tau}} \qquad \text{(eq. 8)}$$

In the preceding equations, the natural frequency (ω_n) provides the settling-time measurement or the loop bandwidth, whereas the damping factor (ζ) gives information about the degree of the loop stability.

The PLL using a simple lag RC filter (See Figure 9) has a disadvantage. From equation (7) and equation (8), (ω_n / ζ) is fixed as $2 \cdot K_{pd} \cdot K_{vco}$ [8]. Thus, the natural frequency, ω_n and the damping factor, ζ cannot be selected independently. Therefore, a PLL design using the simple lag RC loop filter will be constrained by a compromise between ω_n and ζ. However, if a resistor is added in series with the capacitor like shown in Figure 10, then the loop filter transfer function F(s) becomes

$$F(s) = \frac{1 + \tau_2\,s}{1 + \tau_1\,s} \qquad \text{(eq. 9)}$$

where $\tau_1 = (R_1 + R_2)\,C$ and $\tau_2 = R_2\,C$.

The presence of a zero located at $s = -(1 / \tau_2)$ in the loop filter changes the closed-loop transfer function of the type-one, second-order PLL to

$$B(s) = \frac{s\,\omega_n\left(2\,\zeta - \frac{N^2\,\omega_n}{K_{pd}\,K_{vco}}\right) + N\,\omega_n^2}{s^2 + 2\,\zeta\,\omega_n\,s + \omega_n^2} \qquad \text{(eq. 10)}$$

where $\omega_n = \sqrt{\frac{K_{pd}\, K_{vco}}{N\, \tau_1}}$ (eq. 11)

and $\zeta = \frac{1}{2}\sqrt{\frac{K_{pd}\, K_{vco}}{N\tau_1}\left(\tau_2 + \frac{N}{K_{pd}\, K_{vco}}\right)}$ (eq. 12)

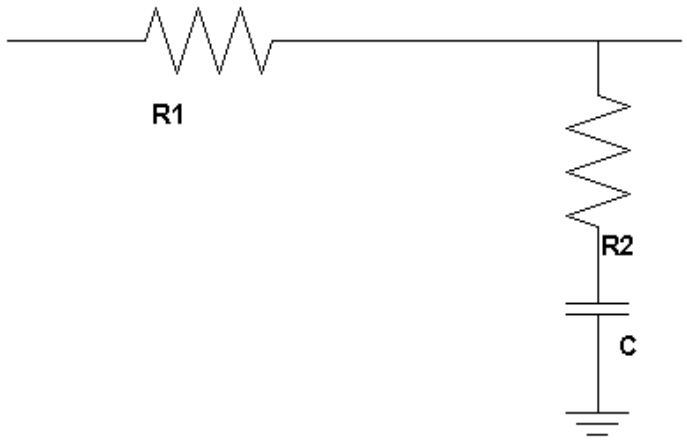


Figure 10. A passive lag-lead low-pass filter

In the above equations, the coupling between the parameters has been greatly relaxed since the two flexible design variables τ_1 and τ_2 determine loop parameters. However, the type-one, second-order loop has a finite DC gain that produces a large, static phase error, which increases the noise susceptibility of the system. Therefore, the finite, static phase error is not desirable.

If having a zero phase error in relations to the step changes in the input frequency is necessary, the DC gain of a loop filter must be infinite. The infinite gain can be accomplished by including a pole at the origin of F(s). The pole at the origin can be obtained by implementing an active loop filter using a large open-loop gain operational amplifier. The transfer function of Figure 11 is given by

$$F(s) = -\frac{1 + s\,\tau_2}{s\,\tau_1} \qquad \text{(eq. 13)}$$

with $\tau_1 = R_1\,C$, $\tau_2 = R_2\,C$

The closed-loop transfer function is given by

$$B(s) = \frac{N\,\omega_n\left(2\,\zeta\,s + \omega_n\right)}{s^2 + 2\,\zeta\,\omega_n\,s + \omega_n{}^2} \qquad \text{(eq. 14)}$$

$$\text{where } \omega_n = \sqrt{\frac{K_{pd}\,K_{vco}}{N\,\tau_1}} \qquad \text{(eq. 15)}$$

$$\text{and} \quad \zeta = \frac{\tau_2\,\omega_n}{2} \qquad \text{(eq. 16)}$$

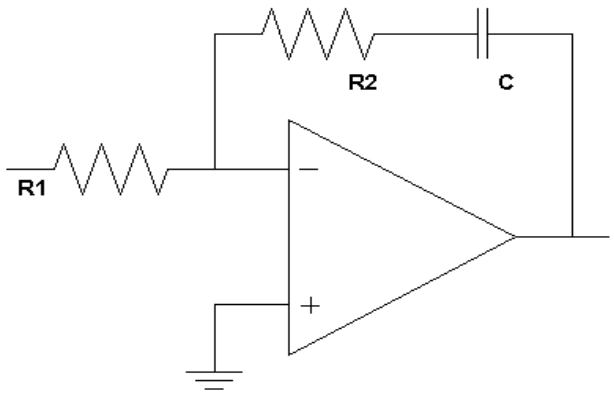


Figure 11. An active low-pass filter

The advantage of an active filter such as shown in Figure 11 over its passive counterpart like a lag RC filter or a passive lag-lead low pass filter comes from the presence of a very high DC gain amplifier, which allows a nearly ideal integration in the loop filter. A filter with a pole at its origin helps to reduce the static phase error to a very small, residual value. Using an active filter, the static phase error of a PLL can be reduced. However, an operational amplifier in the loop filter produces a significant

amount of noise power within the PLL bandwidth. Therefore, the noise power contributes to the offset, which in turn causes unwanted sidebands in the output signal.

A simple way to achieve the same performance result as the active filter with a pole at its origin without using the noisy, offset-susceptible active operational amplifier is to use a charge-pump circuit [9]. When compared with the previously discussed PLLs, the charge-pump PLL offers two important advantages in addition to reducing static phase error. First, the capture range of a charge-pump PLL is only limited by the VCO output frequency range. Second, the static phase error is zero if mismatches and offsets of charge-pump are negligible [22].

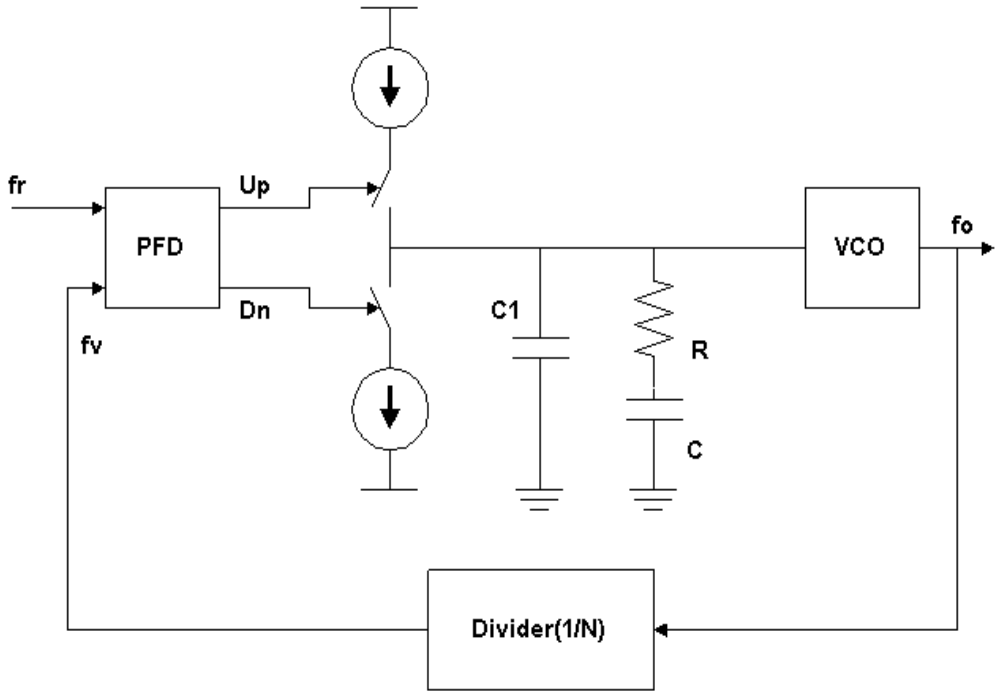


Figure 12. A charge-pump PLL

As in Figure 12, the charge-pump PLL includes a PFD, a charge pump, a LPF that is composed of several capacitors and resistors, a VCO, and a variable frequency divider.

The signals from the PFD, Up and Dn, are used to control the charge-pump circuit. The purpose of the charge-pump circuit is to change the VCO control voltage by applying positive or negative charges to the low-pass filter. The electric current magnitude of the charge-pump PLL is an important factor in the overall loop behavior because it determines the transfer function of the charge-pump circuit that is given by

$$\frac{I_d(s)}{\theta_e(s)} = \frac{I_p}{2\pi} \qquad \text{(eq. 17)}$$

where $I_d(s)$ = the Laplace transform of the average current over a cycle

I_p = the pump current

$\theta_e(s)$ is the Laplace transform of the phase difference at the PFD input

As shown in Figure 12, a simple, second-order passive low-pass filter is composed of a resistor, R and two capacitors, C and C_1.

The transfer function of this filter is given by

$$F(s) = \frac{1 + s\,R\,C}{s^2\,R\,C\,C_1 + s\,(C + C_1)} = \frac{1 + s\,\tau_2}{s\,(C + C_1)\,(1 + s\tau_1)} \qquad \text{(eq. 18)}$$

where $\tau_1 = \left(\frac{C\,C_1}{C + C_1}\right)$, $\tau_2 = R\,C$.

Then, the closed-loop transfer function is found to be

$$B(s) = \frac{K_{pd}\,K_{vco}\left(\frac{1 + s\,\tau_2}{C + C_1}\right)}{s^3 + \left(\frac{1}{\tau_1}\right)s^2 + \left(\frac{K_{pd}\,K_{vco}\,\tau_2}{N\,(C + C_1)}\right)s + \left(\frac{K_{pd}\,K_{vco}}{N\,(C + C_1)\,\tau_1}\right)} \qquad \text{(eq. 19)}$$

And open-loop transfer function $G(s) \bullet H(s)$ is

$$G(s)\bullet H(s) = \left(\frac{K_{pd}\,K_{vco}}{N\,(C + C_1)}\right)\left(\frac{1 + s\,\tau_2}{s^2\,(1 + s\,\tau_1)}\right) \qquad \text{(eq. 20)}$$

According to the definition of type and order, this is a type two, third-order PLL system. In this system, the pole created by capacitor C_1 that is needed to suppress the control voltage ripple coming from the resistor connected in a series must be lower than the reference input frequency in order to attenuate the spurs. But the pole must also be higher than the loop bandwidth; otherwise, the loop will become unstable [35].

The equation (19) can be approximated by a second-order expression to derive outcomes that give an intuitive feel of the transient response. The higher order terms are assumed to be small relative to the lower order terms. The simplified second order expression is given by

$$B(s) \cong \frac{\frac{K_{pd}\,K_{vco}}{N(C+C_1)}\cdot(1+sNCR)}{s^2 + s\left(\frac{K_{pd}\,K_{vco}\,RC}{N\,(C+C_1)}\right)} \qquad \text{(eq. 21)}$$

Therefore, natural frequency and damping factor are given by

$$\omega_n = \sqrt{\frac{K_{pd}\,K_{vco}}{N\,(C+C_1)}} \qquad \text{(eq. 22)}$$

and $$\zeta = \left(\frac{R\,C}{2}\right)\omega_n \qquad \text{(eq. 23)}$$

So, the poles are located at

$$-\zeta\cdot\omega_n \pm j\cdot\omega_n\cdot\sqrt{1-\zeta^2} \qquad \text{(eq. 24)}$$

In the equation (21), the first term in the numerator has primary effects on time frequency response and the second expression has secondary effects because of the zero.

The time frequency response can be obtained using inverse Laplace transformation as in equation (25) where the PLL is initially locked at frequency f_1 and

its oscillation output frequency jumps to f_2 when the counter's modulus value is changed from N to N'.

$$F(t) = f_2+(f_1-f_2)\cdot e^{-\zeta\omega nt}\cdot\left(\cos\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right)+\frac{\zeta-R\cdot C\cdot\omega_n}{\sqrt{1-\zeta^2}}\cdot\sin\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right)\right) \quad \text{(eq. 25)}$$

Since the expression in the large bracket has a maximum value of

$$\frac{1 - 2\cdot R\cdot C\cdot\zeta\cdot\omega_n + R^2\cdot C^2\cdot{\omega_n}^2}{\sqrt{1 - \zeta^2}} \quad \text{(eq. 26)}$$

The lock time is given by

$$\text{Lock Time} = \frac{-\ln\left(\left(\frac{tol}{f_2 - f_1}\right)\cdot\left(\frac{\sqrt{1 - \zeta^2}}{1 - 2\cdot R\cdot C\cdot\zeta\cdot\omega_n + R^2\cdot C^2\cdot{\omega_n}^2}\right)\right)}{\zeta\cdot\omega_n} \quad \text{(eq. 27)}$$

where tol = tolerance of lock-time measurements

And the equation (27) can be approximated by

$$\text{Lock Time} = \frac{-\ln\left(\left(\frac{tol}{f_2 - f_1}\right)\cdot\sqrt{1 - \zeta^2}\right)}{\zeta\cdot\omega_n} \quad \text{(eq. 28)}$$

Figure 13 shows the classical second order model for the transient response derived in the equation (27). The relationship between phase margin, damping factor, and natural frequency is shown in table 2.

In general, theoretical and measured lock times has a difference that is caused by VCO and charge pump non-linearity, VCO input capacitance, and bad capacitor dielectrics that lead to a longer lock time, discrete phase detector sampling effects, charge pump mismatch and leakage, board parasitic factor, and component leakages.

The second order filter in charge-pump PLL has the least thermal noise compared to other types of filters because of its small-sized resistor and the large capacitor next to VCO that minimizes the impact of VCO input capacitance. This filter also has a

maximum resistance to variations in VCO and charge pump gains. If the spur frequency to be filtered is smaller than 10 times the loop-bandwidth frequency, then the second order filter is appropriate. However, if the spur is larger than 10 times the loop bandwidth, then a higher order filter is required [35].

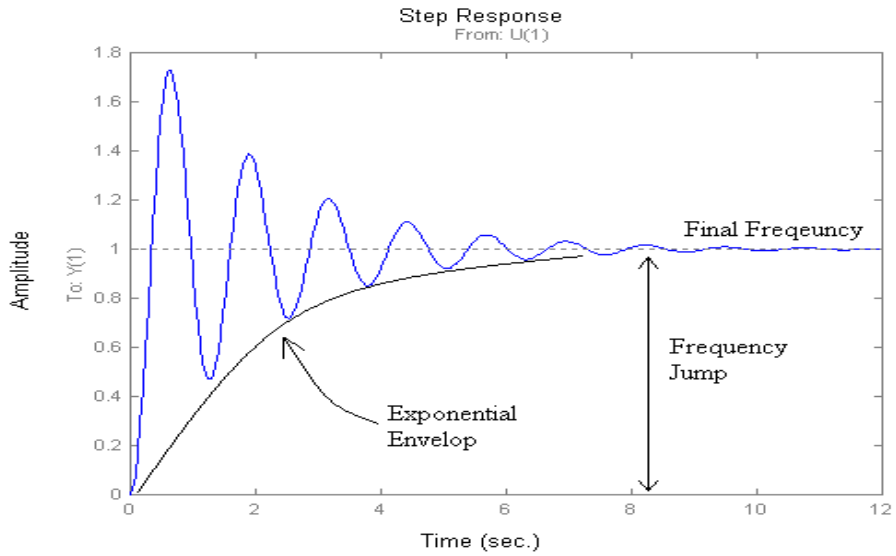


Figure 13. Classical model for the transient response of a PLL

Table 2. Relationship between phase margin, damping factor, and natural frequency

Phase Margin, ϕ	Damping Factor, ζ	Natural Frequency, ω_n
30.00 degrees	0.6580	$0.7599 \cdot \omega_c$
35.00 degrees	0.6930	$0.7215 \cdot \omega_c$
40.00 degrees	0.7322	$0.6829 \cdot \omega_c$
45.00 degrees	0.7769	$0.6436 \cdot \omega_c$
50.00 degrees	0.8288	$0.6033 \cdot \omega_c$
55.00 degrees	0.8904	$0.5615 \cdot \omega_c$
60.00 degrees	0.9659	$0.5177 \cdot \omega_c$
65.00 degrees	1.0619	$0.4709 \cdot \omega_c$
70.00 degrees	1.1907	$0.4199 \cdot \omega_c$

The third order filter in charge pump PLL is shown in Figure 14.

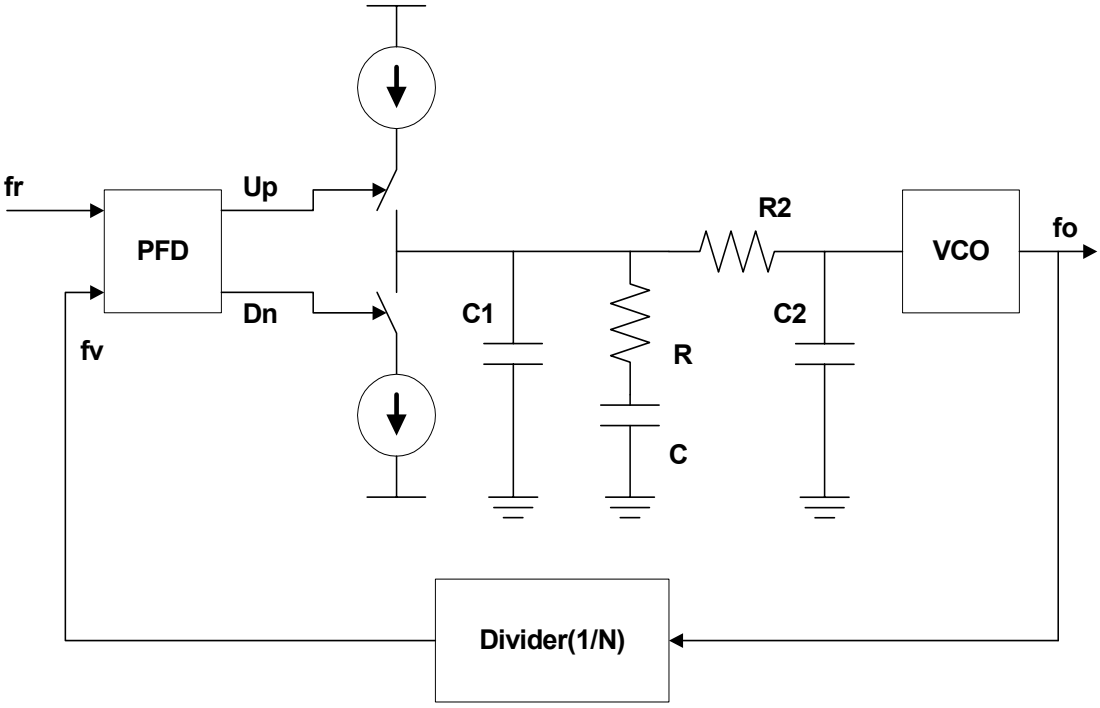


Figure 14. A charge-pump PLL with third-order filter

The impedance of the third order filter is given by

$$F(s) = \frac{1 + s\,R\,C}{s\left(s^2\,R\,R_2\,C\,C_1\,C_2 + s\left(C\,R\left(C_2 + C_1\right) + C_2\,R_2\left(C + C_1\right)\right) + \left(C + C_1 + C_2\right)\right)}$$

(eq. 29)

Then, the closed-loop transfer function is found to be

$$B(s) = \frac{1+sRC}{\left(\frac{NC}{K_{pd}K_{vco}}\right)RC_1R_2C_2s^4 + \left(\left(\frac{N(C+C_1)}{K_{pd}K_{vco}}\right)R_2C_2 + \left(\frac{NC}{K_{pd}K_{vco}}\right)R\left(C_1+C_2\right)\right)s^3 + \left(\frac{N\left(C+C_1+C_2\right)}{K_{pd}K_{vco}}\right)s^2 + RCs + 1}$$

(eq. 30)

With the third order filter, the additional pole must be lower than the reference input frequency to suppress the spurs effectively. However, the pole frequency has to be higher than the loop bandwidth in order to resolve the PLL's stability problem.

Fourth and higher order filters are more practical when the offset frequency spurs to be filtered is at least 20 times the loop bandwidth. However, higher order filters are often unrealistic because the required capacitor values become too small relative to the VCO input capacitance and cause the filters to become unnecessarily complex.

Passive loop filters are generally preferred over active filters as a low pass filter in a charge-pump PLL because of their low cost, simplicity, and low in-band phase noise. An additional in-band phase noise comes from the active device that is used in the loop filter. However, under circumstances where the VCO requires a higher tuning voltage than the PLL charge-pump can handle, active filters are used as a low pass filter. In broadband tuning applications such as those required in cable TV tuners, VCOs commonly require a high tuning voltage. A high tuning voltage is also required for low-noise or high-power VCOs. Many design concepts used in active loop filter charge-pump PLL are analogous to those used in passive loop filter. However, a typical recommendation is to use at least a third order filter to suppress the phase noise coming from the active devices.

The following two types of basic active filters exist: the first type uses the differential charge pump output and the other one uses the single charge pump output pin. In Figure 15, the charge pump active filter that uses a simple gain block is shown as an example of active filter that uses the single charge pump output pin.

This particular architecture involves placing an operational amplifier in front of the VCO. In this architecture, a third or higher order filter should be used to reduce the operational amplifier noise even though spurs are not reduced much as a result. The gain block, -A, in Figure 15 is used to invert the charge pump output, which can be negated by

reversing the charge pump polarity. The gain block is also used to isolate input/output signals and to place a larger capacitor next to the VCO, thereby reducing the impact of the VCO input capacitance and loop filter resistor noise. Sometimes, the architecture in Figure 16 is used to center the charge-pump output voltage at half the charge-pump supply and to lower the spur level by predicting its patterns more accurately.

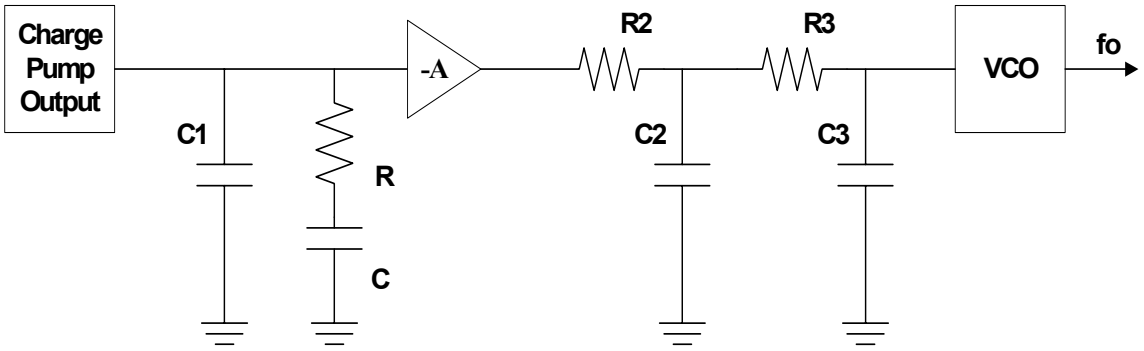


Figure 15. An active filter using the simple gain approach

In general, an architecture that uses the differential charge-pump output is not recommended because it requires an operational amplifier and most PLLs do not have differential output pins.

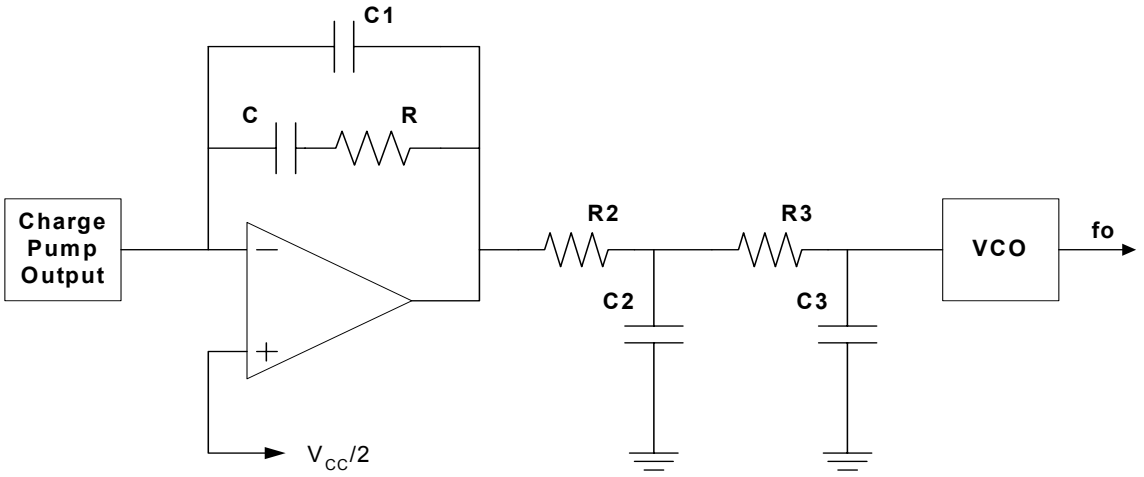
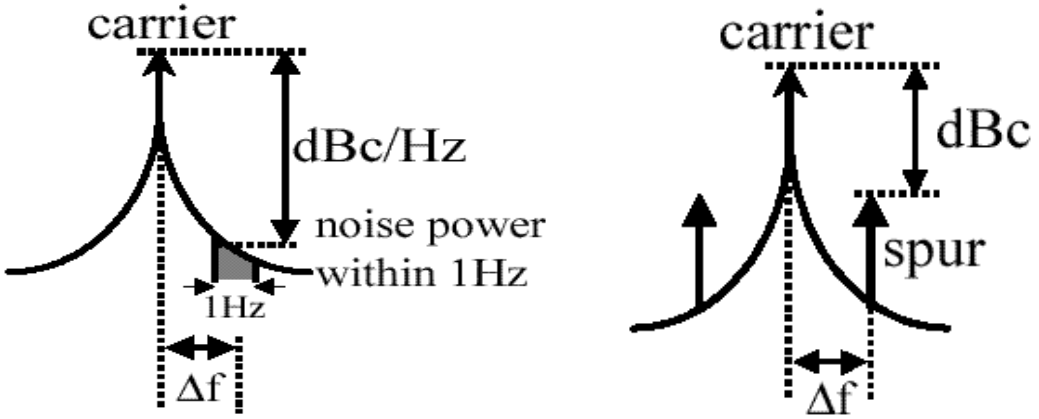


Figure 16. An active filter using the standard feedback approach

2.3 Phase Noise and Spurious Response

A purity of synthesized output signal is the most important requirement in all wireless communication systems. Ideally, this means the frequency synthesizer output should be a pure tone. However, as described in Chapter 1, two different factors (Figure 17) negatively affect the signal purity at the RF output in a PLL-based frequency synthesizer. The first factor is the phase noise associated with physical devices in the PLL. The phase noise limits the quality of the synthesized signal. The noises in the reference, PFD, loop-filter, VCO and frequency divider all contribute in degrading the synthesized signal from an ideal pure sine wave. The other factor manifests itself as relatively high-energy, spurious sidebands. The sidebands have a systematic origin that makes them easier to handle than a fundamental, random noise [2,3].



Phase Noise Spurious tone

Figure 17. Phase noise and spurs in the frequency domain

When an electric current with a fixed frequency gets injected into the loop filter, the resulting spurs become a design issue. The spurs can be grouped into different categories depending on their causes.

The most common type of spur is the reference spur that appears at multiples of the comparison frequency. Usually, spurs are caused by either a leakage or a charge pump mismatch. Depending on their cause, reference spurs may behave differently when the comparison frequency or the loop filter is changed.

At lower comparison frequencies, a dominant cause of reference spurs is a leakage effect. When the PLL is in a locked status, the charge pump will generate short, alternating electric current pulses with long time intervals where the charge pump is tri-stated. When the charge pump is in a tri-state, it has to be high impedance. However, some parasitic leakage will exist through the charge pump, VCO, and loop-filter capacitors. Among these different leakage sources, the charge pump tends to be the dominant one. The charge pump leakage causes FM modulation on the VCO tuning line and produces spurs.

The older PLLs have a large amount of electric current leakage and such leakage used to be the main reason for spurs. Nowadays, the electric current leakage inside PLLs is quite small. Therefore, other factors dominate in creating spurs except at low comparison frequencies. The characteristics of spurs created by factors other than the electric current leakage are determined by the charge-pump turn-on-time for short, alternating pulses. Several factors affect the width of alternating pulses including charge pump mismatch, unequal transistor turn-on-time, dead-zone elimination circuitry, and inaccuracies in the fractional calibration circuitry [54,56].

The charge pump mismatch comes from the mismatching of its sink and source electric currents. If the mismatch is big, then a wider correction pulse is necessary and larger spurs are generated. The unequal turn-on-time are caused by the mobility

difference between P-type and N-type transistors. The elimination circuitry that is used to keep the PLL out of the dead zone causes an additional gate delay at zero-phase error. All these factors make the width of the charge pump correction pulse wider and increase spurs.

To reduce spurs, a high-order loop filter can be utilized to suppress the reference frequency spurs and a much smaller loop bandwidth than the reference frequency can be used. The electric current leakage arising from the charge-pump circuit, loop-filter, varactor diodes, and other components should be reduced in order to achieve low spurs signal. A fully differential configuration will also reduce spurs. Another method for reducing spurs is to use a higher reference frequency adapted in the fractional-N synthesis technique.

Spurs in a frequency synthesizer can be evaluated using the following analysis. Because spurs are caused by the PLL when a signal with an AC component exists in the tuning line of the VCO, the VCO tuning voltage can be described as

$$V_{tune} = V_{DC} + V_{AC}(t) \qquad \text{(eq. 31)}$$

where V_{tune} = VCO tuning voltage

V_{DC} = DC component of tuning voltage in the VCO

V_{AC} = AC component of tuning voltage in the VCO = $V_m \cdot \sin(\omega_m \cdot t)$

ω_m = modulating frequency = comparison frequency

So, the VCO output is given by

$$V(t) = A \cdot \cos(\omega_0 \cdot t + \beta \cdot \sin(\omega_m \cdot t)) \qquad \text{(eq. 32)}$$

where ω_0 = carrier frequency

β = modulation index

Finally, using the Fourier Series for $e^{j\cdot\beta\cdot\sin(\omega m\cdot t)}$, the VCO output can be expressed as

$$V(t) = A\cdot\cos(\omega_0\cdot t + \beta\cdot\sin(\omega_m\cdot t)) \quad \text{(eq. 33)}$$

$$= A\cdot\text{Real}\{\, e^{j\cdot\beta\cdot\sin(\omega m\cdot t)} \sum_{m=-\infty}^{\infty} J_n(\beta)\ e^{j\cdot\beta\cdot\sin(\omega m\cdot t)}\} \quad \text{(eq. 34)}$$

$$= A\cdot\sum_{m=-\infty}^{\infty} J_n(\beta)\cdot\cos(\omega_0\cdot t + m\cdot\omega_m\cdot t) \quad \text{(eq. 35)}$$

From equation (35), the sideband levels can be defined as

Carrier = $J_0(\beta) \approx 1$

First = $J_1(\beta) \approx \beta/2$

Second = $J_2(\beta) \approx \beta^2/8$

The phase noise can be analyzed using a linear, small-signal model of the PLL loop that is shown in Figure 18.

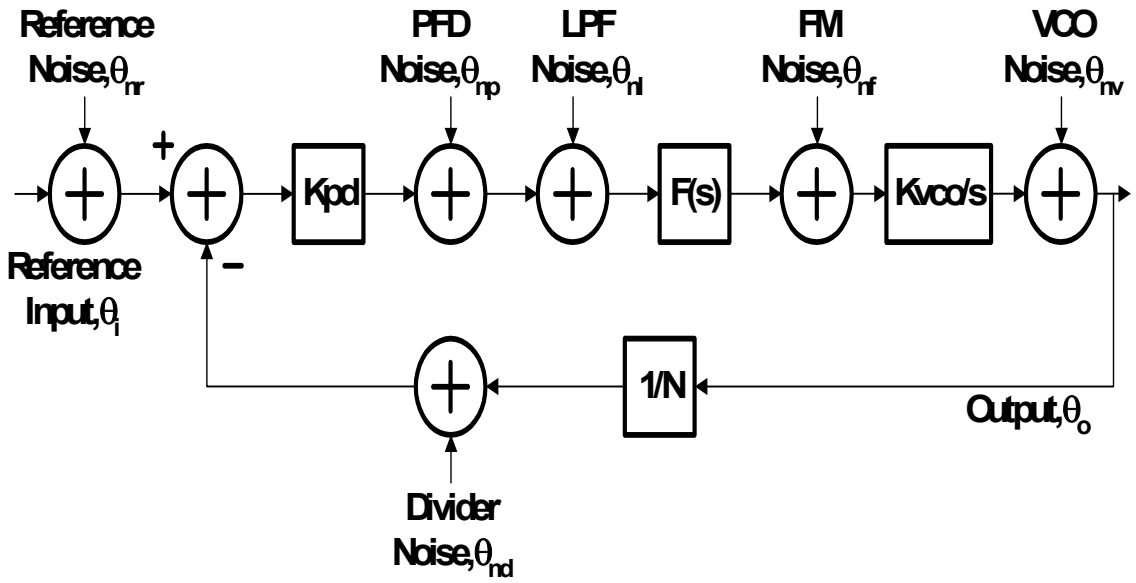


Figure 18. Small signal block diagram of the PLL with noise sources

A PLL that is composed of a phase and frequency detector (PFD), a low pass filter as a loop filter, a VCO, and a divider has many noise sources such as reference

noise, VCO noise, loop filter noise, divider noise, etc. The reference noise (θ_{nr}) is the noise on the reference signal. The PFD noise (θ_{np}) is the noise generated by the Phase and Frequency Detector (PFD). The phase difference signal gets corrupted due to the PFD noise. When a pure electric current switching charge-pump circuit is used, the loop-filter noise (θ_{nl}) arises from the equivalent input noise sources of the amplifier that is used for an active-loop filter, logic circuits, and electric current source noises. The FM noise (θ_{nf}) represents a total noise coming from the pick-up noise at the VCO tuning input node and the VCO power supply noise. The VCO introduces the VCO noise (θ_{nv}) and most of the noise energy is around the oscillator frequency. The divider noise, θ_{nd} is created by the frequency divider [4,45].

In Figure 18, the feed-forward gain (G(s)), feedback gain (H(s)), and open-loop gain (O(s)) are given by

$$G(s) = \frac{K_{pd}\, K_{vco}\, F(s)}{s} \qquad \text{(eq. 36)}$$

$$H(s) = \frac{1}{N} \qquad \text{(eq. 37)}$$

$$O(s) = G(s) \bullet H(s) = \frac{K_{pd}\, K_{vco}\, F(s)}{N\, s} \qquad \text{(eq. 38)}$$

And the transfer functions for various noise sources can be expressed as

$$\text{Crystal reference} = \frac{\theta_{no}}{\theta_{nr}} = \frac{\dfrac{K_{pd}\, K_{vco}}{s}}{1 + \dfrac{K_{pd}\, K_{vco}\, F(s)}{Ns}} = \frac{NO(s)}{1 + O(s)} \qquad \text{(eq. 39)}$$

$$\text{PFD = Loop filter} = \frac{\theta_{no}}{\theta_{np}} = \frac{\theta_{no}}{\theta_{nl}} = \frac{\dfrac{K_{vco}\, F(s)}{s}}{1 + \dfrac{K_{pd}\, K_{vco}\, F(s)}{Ns}} = \frac{N}{K_{pd}} \frac{O(s)}{1 + O(s)} \qquad \text{(eq. 40)}$$

$$\text{FM} = \frac{\theta_{no}}{\theta_{nf}} = \frac{\frac{K_{vco}}{s}}{1 + \frac{K_{pd}\,K_{vco}\,F(s)}{Ns}} = \frac{N}{K_{pd}\,F(s)}\,\frac{O(s)}{1 + O(s)} \qquad \text{(eq. 41)}$$

$$\text{N divider} = \frac{\theta_{no}}{\theta_{nd}} = \frac{\frac{K_{pd}\,K_{vco}\,F(s)}{s}}{1 + \frac{K_{pd}\,K_{vco}\,F(s)}{Ns}} = \frac{NO(s)}{1 + O(s)} \qquad \text{(eq. 42)}$$

$$\text{VCO} = \frac{\theta_{no}}{\theta_{nv}} = \frac{1}{1 + \frac{K_{pd}\,K_{vco}\,F(s)}{Ns}} = \frac{1}{1 + O(s)} \qquad \text{(eq. 43)}$$

If a reference divider, 1/R, generates various reference frequencies, then it also creates a noise that is given by

$$\text{R divider} = \frac{\theta_{no}}{\theta_{nR\_divider}} = \frac{\frac{K_{pd}\,K_{vco}}{s}}{1 + \frac{K_{pd}\,K_{vco}\,F(s)}{Ns}} = \frac{NO(s)}{1 + O(s)} \qquad \text{(eq. 44)}$$

And the noise from the reference signal changes to

$$\text{Crystal Reference} = \frac{\theta_{no}}{\theta_{nr}} = \frac{1}{R}\,\frac{\frac{K_{pd}\,K_{vco}}{s}}{1 + \frac{K_{pd}\,K_{vco}\,F(s)}{Ns}} = \frac{1}{R}\,\frac{NO(s)}{1 + O(s)} \qquad \text{(eq. 45)}$$

Using the equations (36) through (43), the total output phase noise contributed by each noise source can be expressed by

$$\theta_{no}^2 = N^2\,(\theta_{nr}^2 + \theta_{neq}^2)\left(\frac{O(s)}{1 + O(s)}\right)^2 + \theta_{nv}^2\left(\frac{1}{1 + O(s)}\right)^2 \qquad \text{(eq. 46)}$$

where θ_{neq} is the equivalent input noise that is given by

$$\theta_{neq}^2 = \frac{1}{K_d^2}\left(\theta_{np}^2 + \theta_{nl}^2\right) + \frac{1}{K_d^2\,F(s)^2}\,\theta_{nf}^2 + \theta_{nd}^2 \qquad \text{(eq. 47)}$$

In equation (46), the crystal reference noise, PFD noise, N divider noise, FM noise, and loop-filter noise all contain a common factor in their transfer functions. The common factor is given by

$$\frac{O(s)}{1+O(s)} = \frac{1}{N}\frac{G(s)}{1+G(s)\bullet H(s)} \qquad \text{(eq. 48)}$$

All of these noise sources are referred to as in-band noise sources. If the loop bandwidth (ω_c) and phase margin (ϕ) are defined as [3]

$$\left|\left| G(j\cdot\omega_c)\cdot H \right|\right| = 1 \qquad \text{(eq. 49)}$$

$$180 - \angle\, G(j\cdot\omega_c)\cdot H = \phi \qquad \text{(eq. 50)}$$

Then, equation (48) can be approximated by

$$\frac{O(s)}{1+O(s)} = \frac{1}{N}\frac{G(s)}{1+G(s)\bullet H(s)} \approx \begin{cases} 1 & \text{For } \omega << \omega_c \\ \dfrac{G(s)}{N} & \text{For } \omega >> \omega_c \end{cases} \qquad \text{(eq. 51)}$$

Therefore, this term (Equation 51) has a low pass transfer function. So, the PLL functions as a low-pass filter for phase noise arising in the crystal reference noise, PFD noise, N divider noise, FM noise, and loop filter noise. However, the VCO noise is multiplied by a different transfer function

$$\frac{1}{1+O(s)} = \frac{1}{1+G(s)\bullet H(s)} \qquad \text{(eq. 52)}$$

And this transfer function can be approximated by

$$\frac{1}{1+O(s)} = \frac{1}{1+G(s)\bullet H(s)} \approx \begin{cases} \dfrac{N}{G(s)} & \text{For } \omega << \omega_c \\ 1 & \text{For } \omega >> \omega_c \end{cases} \qquad \text{(eq. 53)}$$

So, the equation 53 represents a high-pass filter for phase noise generated in the VCO. The transfer function of equation (51) is shown in Figure 19 and the transfer function of equation (53) is shown in Figure 20.

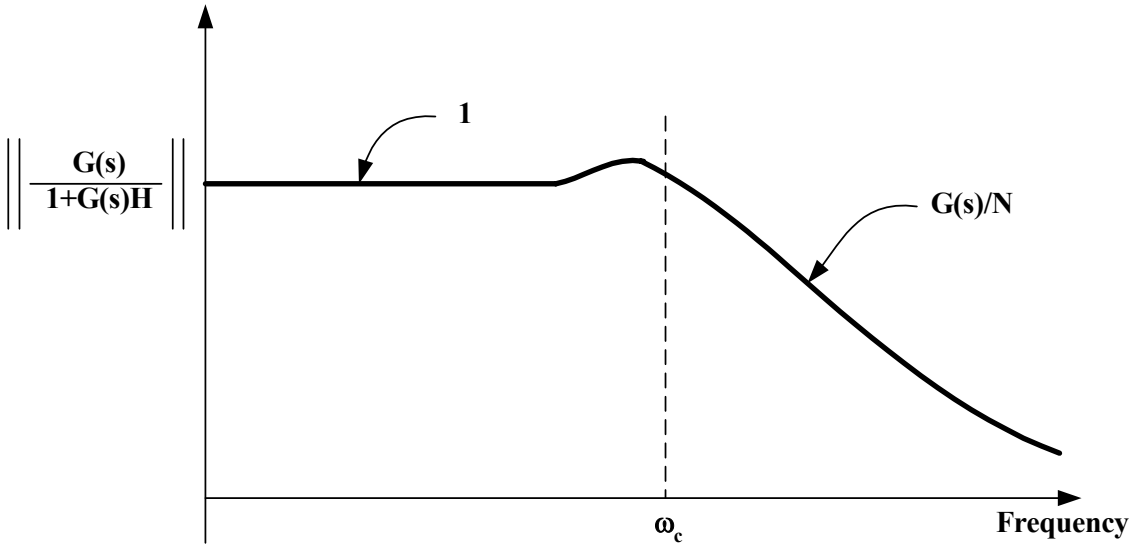


Figure 19. Transfer function multiplying all in-band noise sources

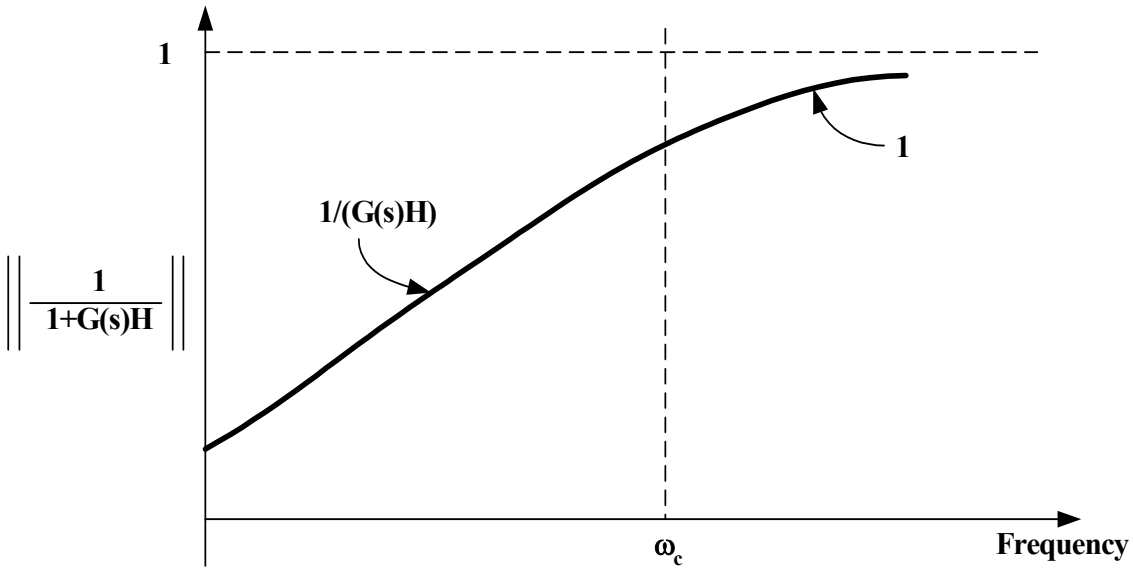


Figure 20. Transfer function multiplying the VCO noise

The results in the preceding sections come from the fact that the VCO is an emulated integrator with respect to the phase information that functions as a low-pass filter. Therefore, the loop bandwidth should be as wide as possible in order to minimize the output phase noise caused by the VCO inherent phase noise θ_{nv}. However, in order to achieve a minimum phase noise from the in-band noise sources, the loop bandwidth should be as narrow as possible while minimizing the in-band noise contributed by the other loop components. In addition to the conflict between the in-band noise sources and the VCO inherent noise, the loop bandwidth is further confined by the fact that the loop bandwidth needs to be less than the reference input frequency to keep the loop stable and to suppress the spurs at the output. Therefore, to attain a minimal phase noise performance from in-band noise sources and VCO inherent noise, the best place to put the loop bandwidth is where the VCO phase noise crosses the reference phase noise times N.

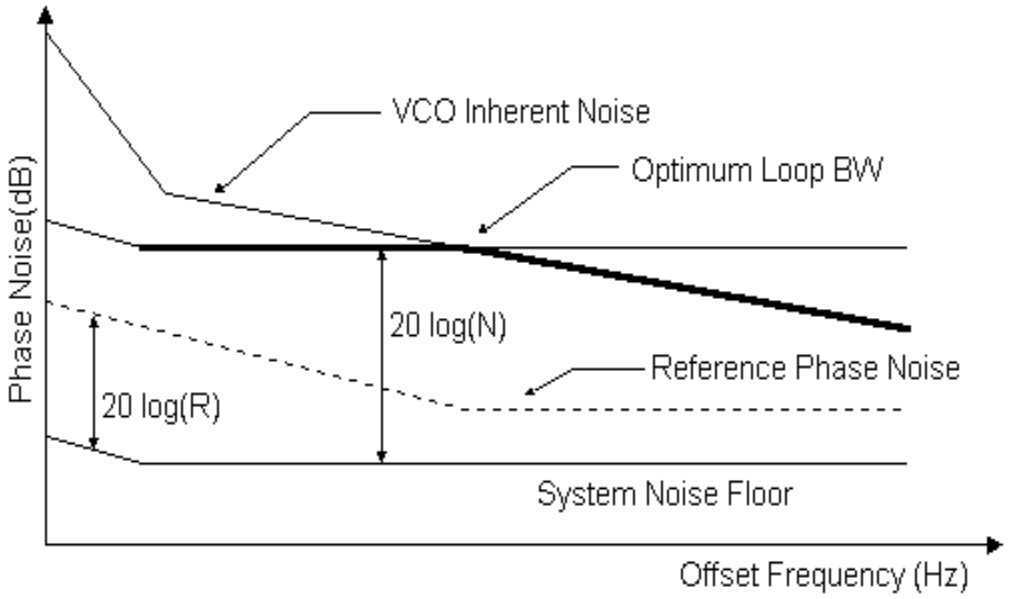


Figure 21. Optimal loop bandwidth of a PLL

This graphical estimation of the PLL's optimal loop bandwidth for achieving a minimum phase noise is shown in Figure 21. The optimal loop bandwidth is determined based on the following considerations: the phase noise inside the loop bandwidth should not be less than the in-band noise multiplied by N and the phase noise outside the loop bandwidth should not be less than the VCO inherent noise [19].

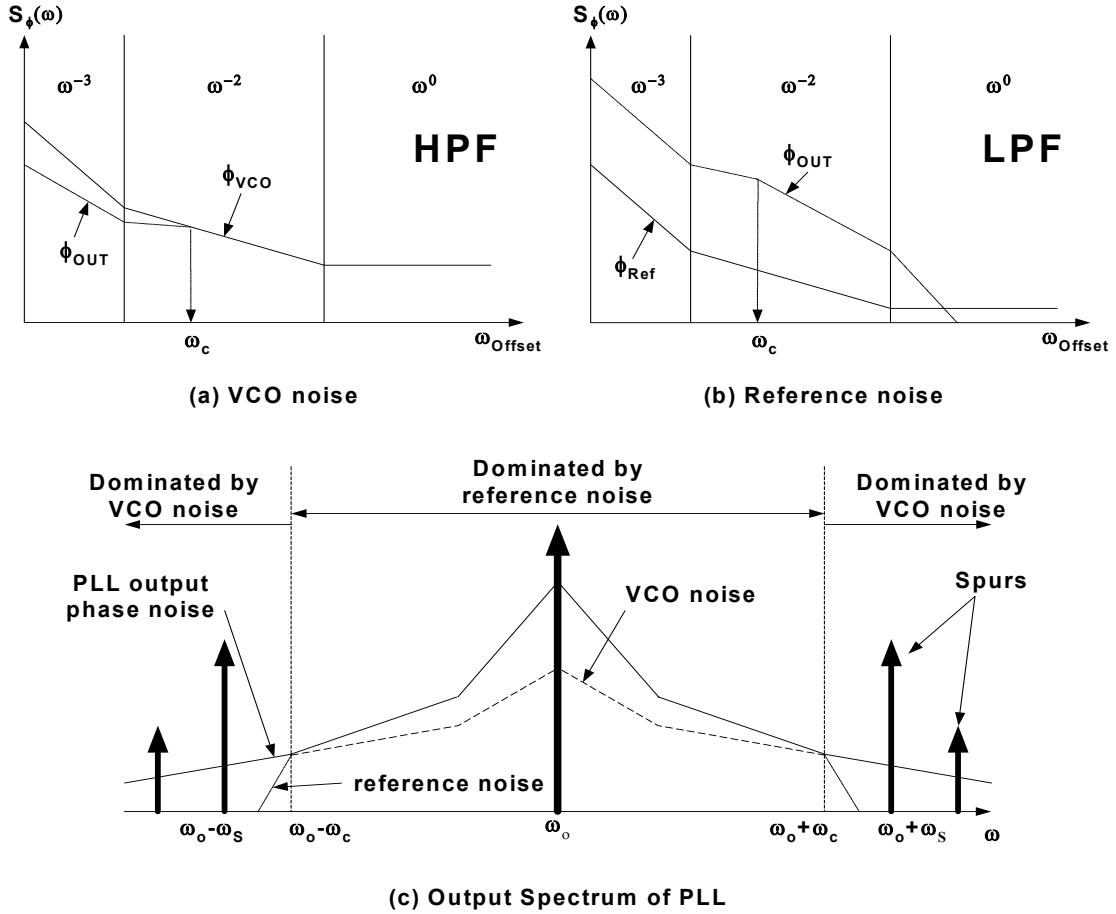


Figure 22. Phase noise transfer functions in a PLL synthesizer (a,b)

typical phase noise and spurs spectral plot (c)

A several other factors such as the following could have an impact on the phase noise: in-band VCO phase noise contribution, lower charge pump gain phase noise adjustment, dual PLL adjustment, noisy crystal reference consideration, resistor noise, and input

sensitivity violation problem. For example, the VCO actually does contribute noise within the loop bandwidth in Figure 20. Specifically, the VCO tends to produce more noise within the loop bandwidth in case of a narrow bandwidth or a noisy VCO.

In Figure 22, the details of a PLL synthesizer's phase noise transfer functions based on Leeson's equation, and its typical phase noise and spurs spectral waveforms are shown.

2.4 Conclusion

In this chapter, an overview and modeling of PLLs have been presented. A PLL that is composed of a PFD, a loop filter, a divider, and a VCO is a negative feedback system that operates on the excess phase of periodic signals. The signals at various points of a typical PLL that has only a small phase difference between the input and output signals have been discussed.

Generally, a PLL is a non-linear device because of the N divider, PFD, and prescaler. However, the PLL can be assumed to be a linear device if the loop is in a locked status when the reference frequency is at least 10 times larger than the loop bandwidth. With this linear approximation, a several transfer functions including open loop and closed loop transfer functions, natural frequency, and damping factor have been derived using a simple servo control theory.

The effects of loop filters on the PLL performance have been considered. A simple way to reduce static phase error without an increased noise from the active device is a charge-pump PLL with passive loop filter. So, the charge-pump PLL architecture and its functional characteristics have been analyzed.

Finally, the optimal point of the loop bandwidth where the overall noise from in-band and VCO inherent noises is minimum has been discussed based on the characteristics of several phase noise and spur sources.

Chapter 3

Frequency Synthesizer Architectures

To implement a complete transceiver for wireless communication systems, a crucial building block that generates the local oscillator (LO) signal is required by both the receiver and the transmitter. This local oscillator signal-generating block is the frequency synthesizer. Wherever frequencies are translated, the frequency synthesizer is crucial for providing a clean, stable and programmable local oscillator signal. The frequency synthesizer needs to be programmable in order to address all frequency channels and be fast switching to perform the addressing sufficiently fast. The signal generated from the frequency synthesizer should be clean because a low oscillator noise is vital for a high-quality and reliable information transfer.

Generally, frequency synthesizers can be categorized into three groups: the table-look-up synthesizer, the direct synthesizer, and the indirect or phase-locked loop synthesizer [45]. The table-look-up synthesizer or digital synthesizer generates the sinusoidal signal piece by piece using digital values of the waveform stored in memory. The direct synthesizer synthesizes the wanted output frequency from a single reference by multiplying, mixing, and dividing. The indirect frequency synthesizer creates its output by phase-locking the divided output to a reference signal.

In the following sections, the details of the three types of frequency synthesizer architectures including their working theories, advantages, and disadvantages will be

discussed. First, the table-look-up synthesizer and the direct synthesizer will be covered. Then, the PLL-based frequency synthesizers will be discussed.

3.1 The Table-look-up and Direct Synthesizers

A straightforward way to implement a frequency synthesizer is the direct synthesizer that is also known as brute-force method shown in Figure 23. A large number of crystal sources are used to synthesize a specific number of frequencies individually. Other frequencies can be generated through a combination of multiplying, dividing, mixing, and filtering operations. By repeatedly mixing and dividing crystal output signals, an accurate frequency is attainable. Theoretically, the output spectrum will also be as clean as the reference spectrum and fast frequency hopping will be possible. However, when implementing the direct synthesizer, cross-coupling between stages is a serious problem for the spectral purity and the large number of components causes the synthesizer to be very bulky and power hungry. Another obvious drawback associated with the direct synthesizer is high costs [8,9,45].

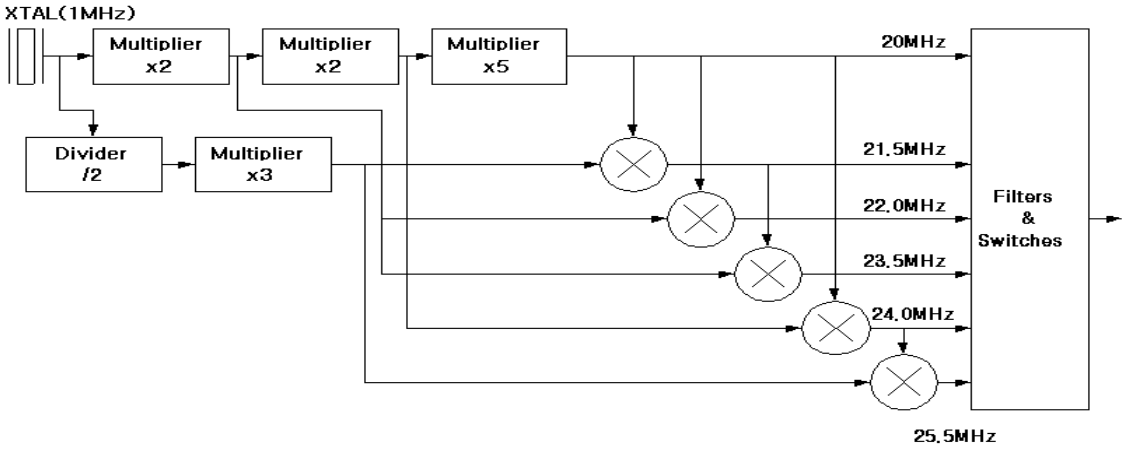


Figure 23. A direct synthesizer example

The table-look-up synthesizer is one of the other frequency synthesizer implementation methods [5]. The hardware needed in a table-look-up synthesizer are a digital accumulator whose capacity determines the frequency resolution, a memory containing a cosine, a Digital-to-Analog Converter (DAC), and a low-pass filter for removing high-frequency spurs. This technique relies on a large number of digital samples taken from a very low-frequency cosine or sine wave for its operation. This low-frequency cosine wave is the system step frequency that determines the resolution of the table-look-up synthesizer. The digital samples are stored in a Read-Only Memory (ROM) and are taken out at regular time intervals set by a reference clock. Then, high frequencies can be generated by taking a fewer samples that are further separated from the ROM look-up table. Figure 24 shows a functional block diagram of table-look-up synthesizer. The accumulator adds the frequency-setting data to its previous contents once every clock cycle. Then, the output value of accumulator is used to address the ROM look-up table. Next, the address decoding circuitry of the ROM selects the corresponding samples. The samples are then fed to the DAC. The DAC converts the digital data to an analog signal and the LPF smoothes out the analog signal [10,48,59].

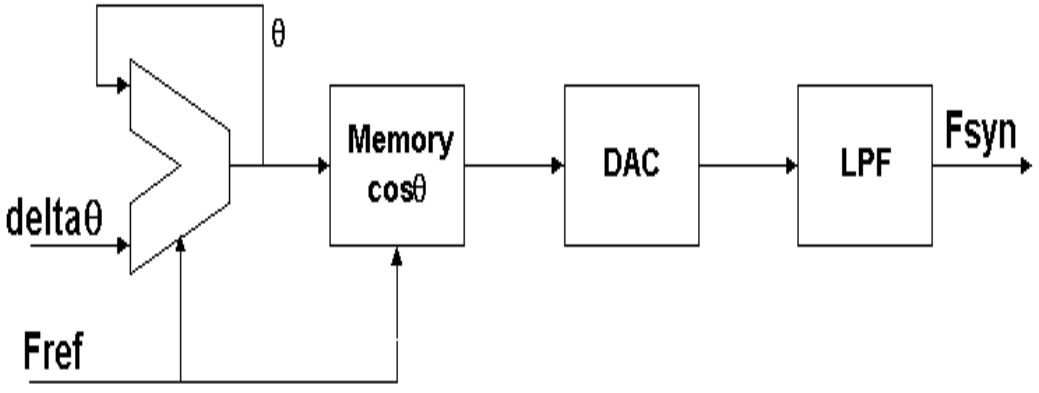


Figure 24. A table-look-up synthesizer

In this architecture, the frequency control is achieved by changing the value of the frequency-setting data. A larger value forces the accumulator to take bigger phase steps every clock cycle. The larger phase steps result in the ROM being scanned in less time. Therefore, the larger the frequency word, the higher the frequency. This method can achieve a fine frequency resolution and a fast frequency-locking speed. However, it can't be directly used in wireless communications operating at a frequency of several GHz because of its high power consumption and the highest-frequency limitation imposed by the Nyquist sampling theorem [6,7,8,9]. Additionally, a high clock frequency is required to cover a wide bandwidth that leads to high power consumption. Moreover, high-frequency spurious tones tend to corrupt the spectral purity. Thus, a table-look-up synthesizer is usually combined with a fixed-frequency Phase-Locked Loop (PLL) frequency synthesizer to extend the highest-frequency limitation [10]. This combined synthesizer is called as Direct Digital Frequency Synthesizer (DDFS).

An example of this DDFS is shown in Figure 25. In this figure, a rather low-frequency signal F_{low} is generated using a table-look-up synthesizer, which is then up-converted to the desired RF frequency with a fixed-frequency oscillator signal F_{IF}. The fixed high-frequency oscillator signal is generated using a lower reference frequency from a PLL-based synthesizer. Thus, the output frequency is given by

$$F_{out} = F_{low} + F_{IF} \qquad \text{(eq. 54)}$$

The main advantage of this architecture is the fixed frequency of the PLL synthesizer. Because the reference choice is free, the loop bandwidth can be optimized for noise reduction. Besides reduced noise, the frequency can be changed rapidly by changing the frequency of F_{low}. However, this architecture suffers from the limited frequency range

because of the low F_{low}, which can only be increased by making a faster DAC. Depending on the required spectral purity of the synthesized signal, the DAC needs a large number of bits and will therefore already be power-hungry. Therefore, the DDFS will only be useful in systems that require very fast frequency hopping. The flexibility of this architecture can be expanded by replacement of the table-look-up synthesizer with another PLL. This results in the so-called dual-loop indirect frequency synthesizer that has more degree of freedom than the standard PLL architecture [12,44]. The details will be covered in the following section.

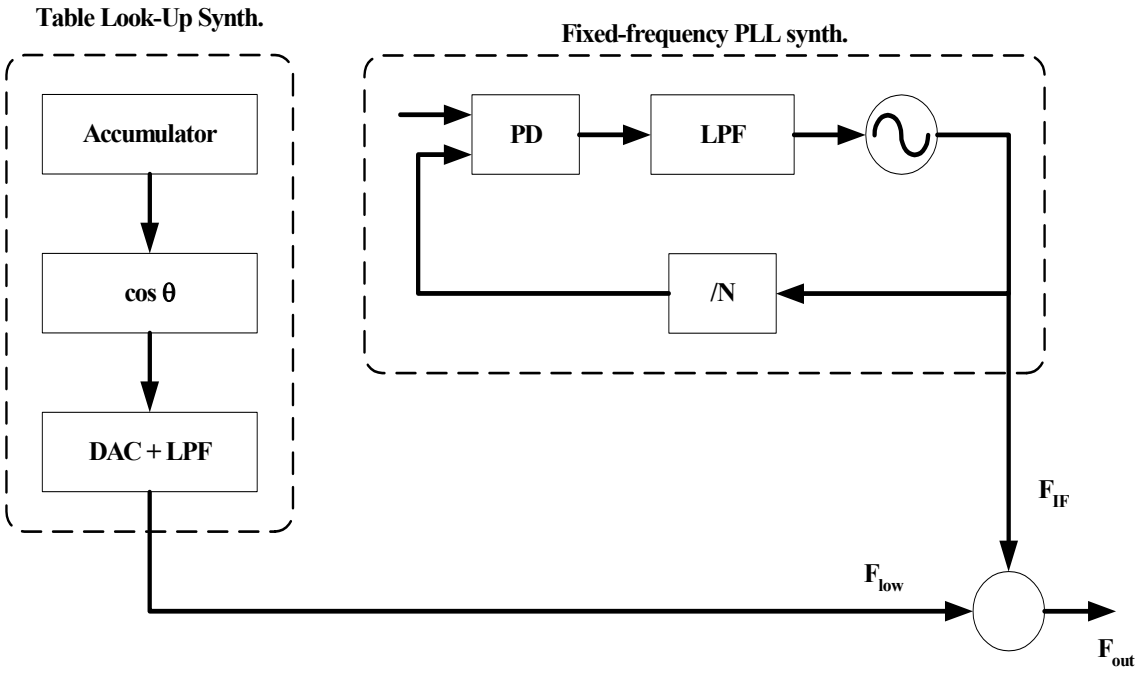


Figure 25. A direct digital frequency synthesizer

3.2 The Indirect or PLL-based Frequency Synthesizer

The PLL-based or indirect frequency synthesizer consists of three basic components: a phase detector, a loop filter, a voltage controlled oscillator and optionally

a frequency divider. The phase detector compares the phase of the input signal against the phase of the VCO. The output of phase detector is a measure of the phase difference between the two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage on the VCO changes the frequency in the direction that reduces the phase difference between the input signal and the local oscillator. The PLL-based frequency synthesizer generates its output by phase-locking the divided output to a reference signal [11]. The simplest form of a PLL-based frequency synthesizer is shown in Figure 26.

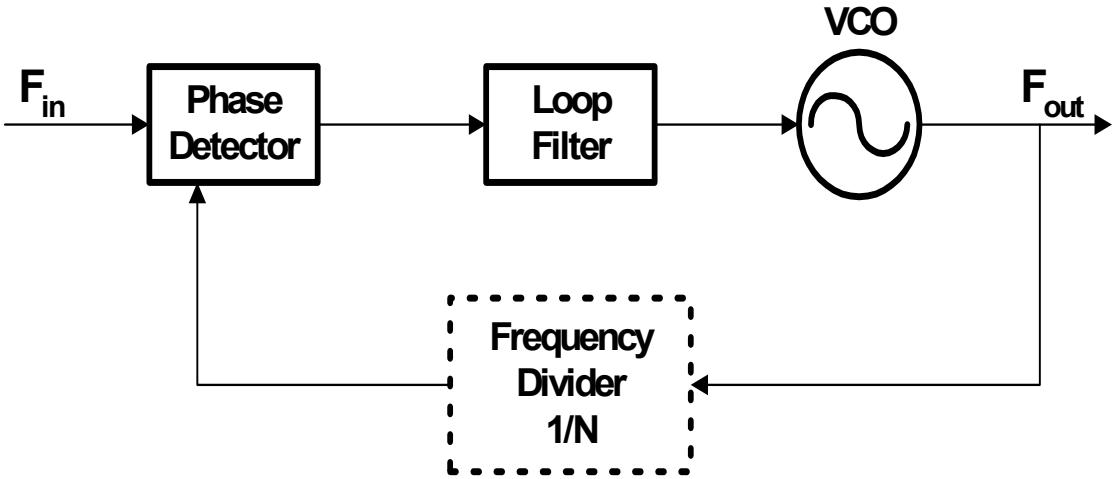


Figure 26. A simple frequency synthesizer

The phase-locked loop frequency synthesizer has the potential of combining high frequency and low power. However, its most distinct advantage is that the phase-locked loop is very well suited for integration in low-cost IC processes, like CMOS. This is the reason why the PLL is used for frequency synthesis in almost all wireless communication chip sets on the market [11]. In other words, the advantages of the PLL are low cost, effective spurious-noise suppression, and low power dissipation. One of the major

disadvantages is that both the fine frequency resolution and the low phase noise can be achieved only in complecate implementations. In fact, the primary deficiency of the PLL is the inverse relationship between the step size and the phase noise. As the step size decreases, division ratios in the system must increase. The higher the division ratio, the worse the phase noise within the loop bandwidth close to the center frequency. Another drawback is a slow switching speed from one frequency to another because of the negative-feedback loop dynamics.

Among PLL-based frequency synthesizers, charge-pump PLL frequency synthesizers are the most popular because of their simplicity, low manufacturing cost, and low power dissipation as well as reduced static phase error.

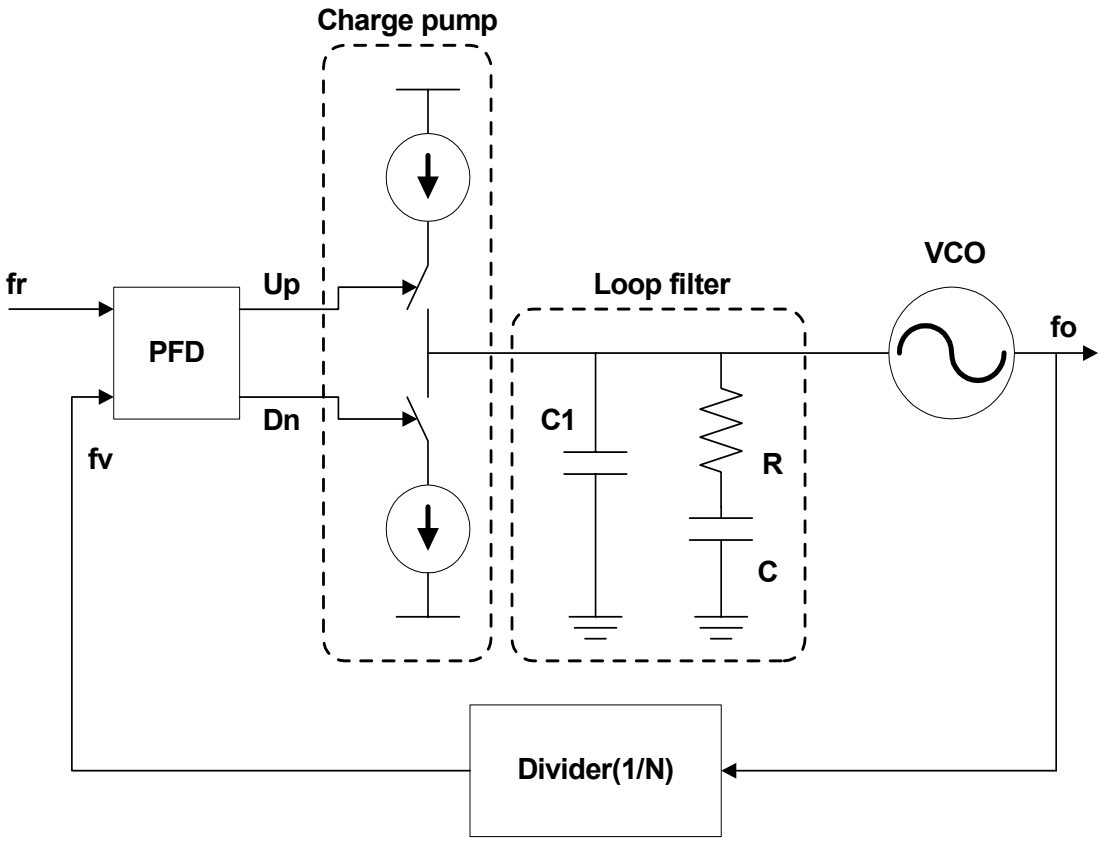


Figure 27. A simple charge-pump PLL

As shown in Figure 27, a charge-pump method can be combined easily with a Phase Frequency Detector (PFD) and passive loop filter to form a type-two, third order system. But this charge-pump PLL frequency synthesizer has some problems, such as low locking-time speed, large time constant requirement, and non-linearity of integrated Voltage-Controlled Oscillator (VCO).

In the frequency synthesizer, a large loop bandwidth is desired to achieve a fast dynamic response, but the selection of loop bandwidth is constrained by the closed loop stability and phase-noise requirements. If a charge-pump PLL has two dominant poles, the loop bandwidth must satisfy the following equation [33]:

$$\omega_n < \frac{\omega_{ref}}{\sqrt{\pi\left(RC\omega_{ref} + \pi\right)}} \qquad \text{(eq. 55)}$$

From equation (55), the maximum loop bandwidth is limited by the reference frequency because of the stability problem. In general, the reference frequency is 10 times larger than the loop bandwidth. The loop bandwidth of a frequency synthesizer is also limited by the phase-noise requirement. There is an optimum loop bandwidth that minimizes the total noise power coming from the noise sources of a PLL as discussed in earlier chapter. However, the optimum loop bandwidth may fail to fulfill the fast locking-time requirement because it depends on all noise sources of the frequency synthesizer.

A classical charge-pump PLL-based frequency synthesizer needs a large time constant to stabilize the system. If a large resistor is used to get the large time constant, the noise power increases. On the other hand, a large capacitor cannot be easily implemented using Integrated Circuit (IC) technology and also increases the manufacturing cost and power consumption.

Usually, the integrated LC VCO has a non-linear characteristic. And the non-linear characteristic can degrade the PLL transient performance and destabilize the closed-loop system [49]. The effects of such problems can be reduced using a complex linearization method, but this method also increases design complexity and manufacturing cost.

A dual- or multi-loop frequency synthesizer is one of the recently developed methods. In this method, a mixer is incorporated into the PLL, as shown in Figure 28. The method can alter the relationship between the channel spacing and the reference frequency of integer-N synthesizers by employing two or more loops. There are mainly two types of dual-loop synthesizers [44]. Both types connect two PLLs using a Single Side Band (SSB) mixer. However, one type connects the PLLs in parallel and the other type in serial. The basic idea is to add a low variable frequency to a high, fixed offset-frequency. Therefore, the frequency change of the synthesizer can be obtained by changing the division ratio in the low-frequency loop.

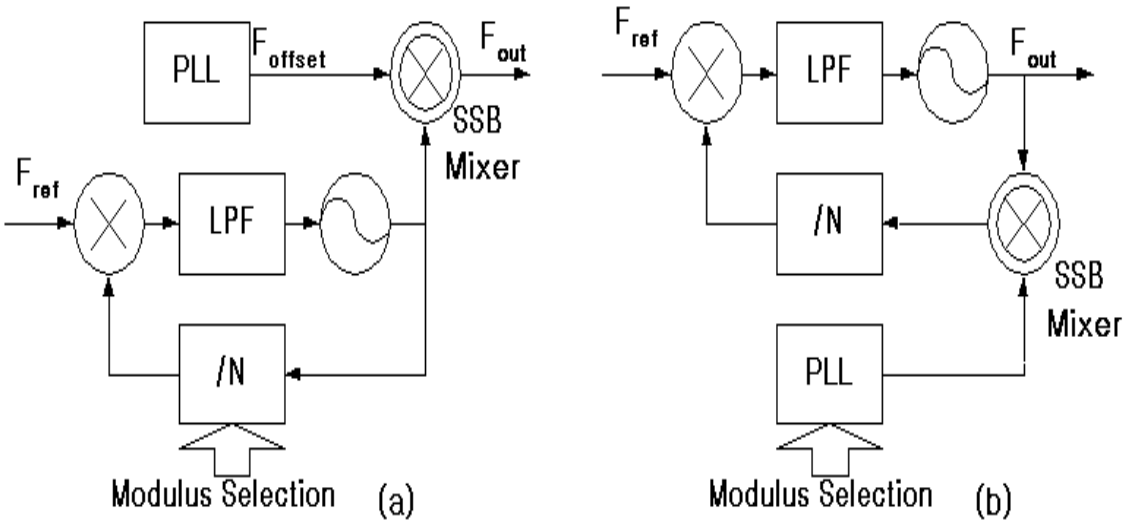


Figure 28. A dual-loop architect frequency synthesizer

In Figure 28(a), the fixed frequency is mixed with the variable frequency by the SSB mixer at the output. Thus, it suffers from large spurs. In Figure 28(b), a variable frequency is added inside the loop. Although this configuration needs more time to settle, the sideband from the mixer can be greatly attenuated by the loop filter. The advantage of this architecture over integer-N topologies is that the loop bandwidth can be large. Because the VCO in the high-frequency loop operates at a higher frequency, the phase-noise performance is expected to be worse than that in a low-frequency loop. Therefore, a larger loop bandwidth can provide more reduction of the phase noise close to the carrier. Moreover, the division number of the divider is also reduced because of the fixed offset-frequency. However, the dual-loop frequency synthesizer has the sidebands produced from non-ideal SSB mixing and consumes more power than the single-loop method [12].

As discussed earlier, the PLL-based frequency synthesizer generates its output by phase-locking the divided output to a reference signal. So, categorizing frequency synthesizers based on their dividing methods is one of the most popular methods in grouping PLL-based frequency synthesizers. The simplest form of a synthesizer that is categorized by dividing methods is shown in Figure 29.

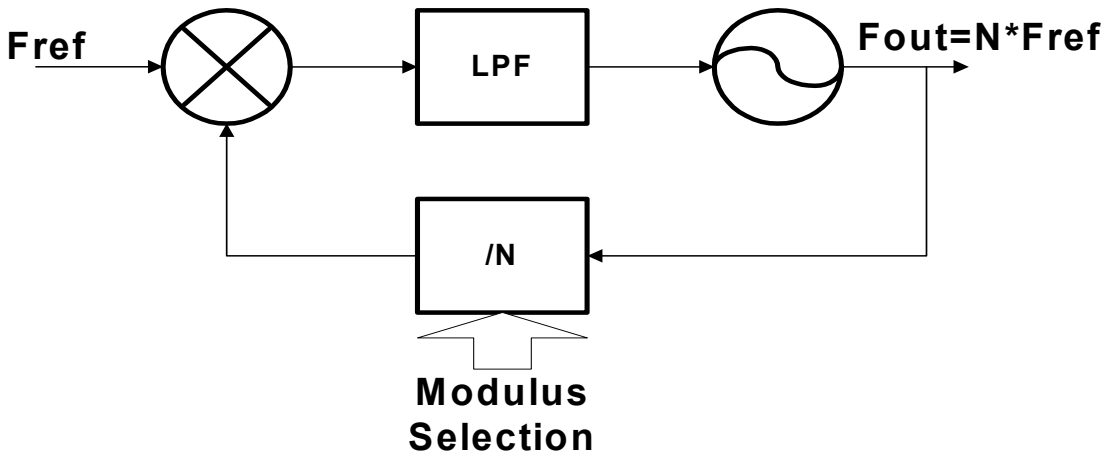


Figure 29. An integer-N frequency synthesizer

In this integer-N architecture, the feedback frequency, f_o/N, equals the input reference frequency f_{ref}. Thus, the output frequency is given by $f_o = N \cdot f_{ref}$. In general, f_{ref} is fixed. So, the frequency step or spacing is equal to the reference frequency and the various frequencies are obtained by changing the modulus number, N. Therefore, to achieve small channel spacing, a low f_{ref} is needed. This low f_{ref} mandates a narrow loop bandwidth to block the signal components at f_{ref} and its harmonics. However, small loop bandwidth results in an increased settling time of the frequency synthesizer and reduces VCO noise suppression potential of the PLL. This low reference requires the VCO frequency to be divided by a large integer N. So, this large divider value results in increased in-band phase noise of the VCO signal in dB by an amount of $20 \cdot \log N$ from the equation (46). Thus, this simple integer-N frequency synthesizer is not suitable for the wireless communication systems that require low phase noise, fast switching time, and narrow frequency spacing [22].

If the desired output frequency exceeds the maximum clock frequency of the programmable divider in integer-N frequency synthesizer, this problem can be overcome by adding a prescaler preceding the programmable divider as shown in Figure 30.

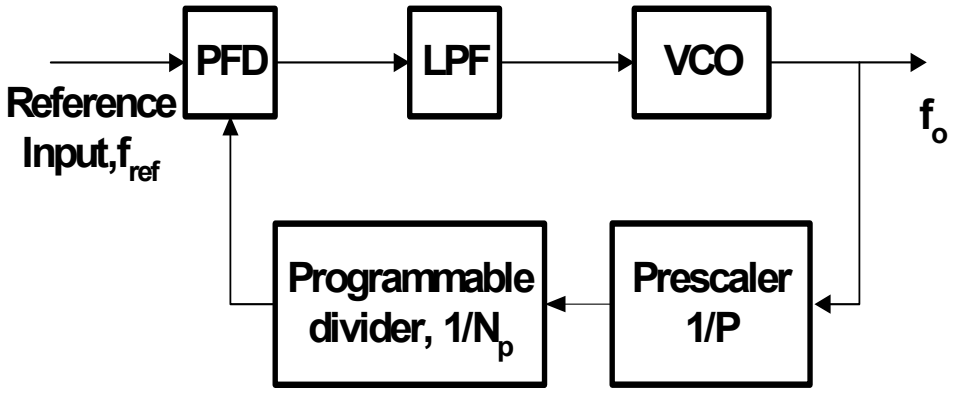


Figure 30. A frequency synthesizer with a single modulus prescaler

If this system is in a locked status, the output frequency, f_o, is given by $f_o = N_p \cdot P \cdot f_{ref,}$ where N_p is the divider ratio of the programmable frequency divider and P is the fixed divider ratio of the prescaler and the frequency spacing is set by $P \cdot f_{ref}$. So, higher frequency operation is allowed. However, it does so at the expense of either increased frequency channel spacing or decreased reference frequency. Therefore, this architecture can cause increased lock-on time and sidebands in the system that needs decreased reference frequency to support specific channel spacing.

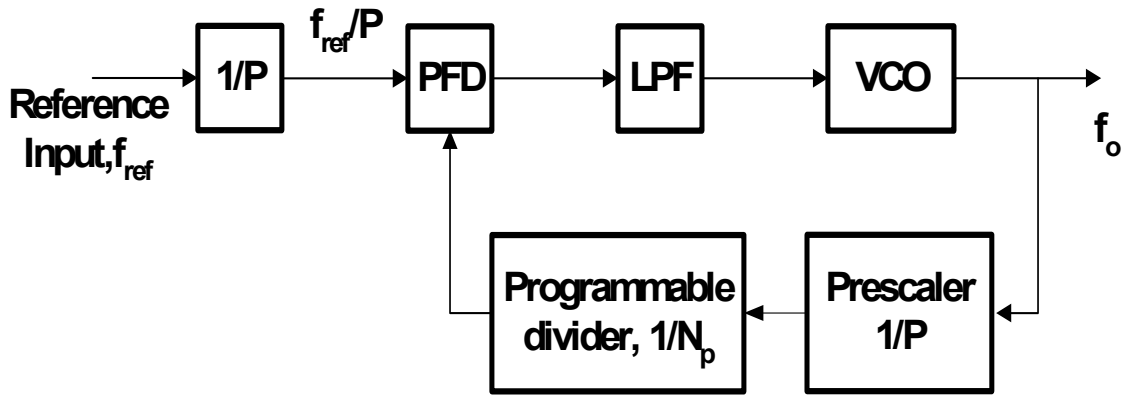


Figure 31. A frequency synthesizer with a prescaler

This channel spacing problem can be solved using the architecture that is shown in Figure 31 since the output frequency of this frequency synthesizer changes by the desired frequency spacing, f_{ref}. However, this method also causes other problems that result from narrowing the loop bandwidth to suppress the reference frequency leakage.

The solution to the frequency resolution problem is the Dual-Modulus Prescaler (DMP). The dual-modulus prescaler is able to divide by N_p and $N_p + 1$ with some additional logic. The additional logic causes some delay in the circuit, reducing its operation speed. By combining the dual-modulus prescaler with proper programmable

counters, a programmable high-frequency divider can be constructed as shown in Figure 32. The full divider consists of a DMP, a programmable counter P, and a swallow counter S. The DMP divided by (N_p + 1) and the S-counter counts the output pulses, until a number S is reached. Then, it changes the DMP modulus control bit, resetting the prescaler division to N_p. The P-counter also counts the DMP output pulses, until a number P is reached. Then it resets both S-counter and P-counter and then the division process is restarted. Therefore, the overall division number becomes

$$N = (N_p + 1) \cdot S + N_p \cdot (P - S) = P \cdot N_p + S \qquad \text{(eq. 56)}$$

because during one output period of the full divider, the DMP has divided S times by (N_p + 1) and (P – S) times by N_p. If S is a variable between 0 and (N_p – 1), a complete range of division numbers can be realized. For a proper reset by the P-counter, P must be larger than the largest value of S. For a given minimum synthesizable frequency, the prescaler division number is limited because the smallest obtainable division number is $N_{min} = N_p^2$.

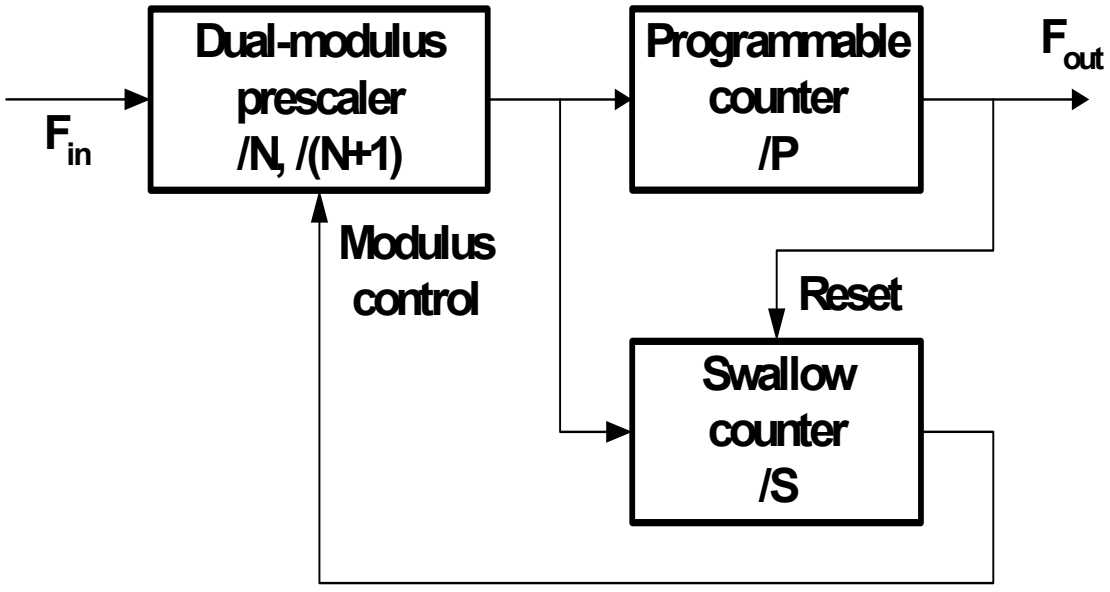


Figure 32. A full frequency divider with a dual-modulus prescaler and two counters

From equation (56), the frequency step size or frequency spacing of the synthesizer using the dual-modulus prescaler equals the PFD reference frequency input. However, trade-offs exist between the loop bandwidth and loop performance.

Another way to implement a frequency synthesizer is the fractional-N method [13,14,15]. The fractional-N frequency synthesizer does not require additional currents, circuit complexity, or larger dies than the other methods [18]. In this structure, the reference frequency, f_{ref}, can be many times the frequency step time (f_{step}) because the output frequency of the PLL (f_{vco}) is given by

$$f_{vco} = f_{ref}\left(N + \frac{K}{F}\right) \qquad \text{(eq. 57)}$$

where F is the fractional portion of the average division ratio and K is the accumulation constant. In equation (57), the frequency division ratio for the dual modulus frequency divider (N/N+1) comes from

$$N_{fractional} = \frac{N * (F - K) + (N + 1) * K}{F} = N + \left(\frac{K}{F}\right) \qquad \text{(eq. 58)}$$

with $F \geq K \geq 0$. Using the fractional-N frequency synthesizer, the phase noise is theoretically improved by $20 \cdot \log(F)$. However, in actual practice, the improvement is limited by additional narrow filtering and phase noise contributed by the PFD [16].

On the hardware level, the fractional part (K / F) can be obtained from a digital accumulator of size F in Figure 33. The accumulator is clocked at the frequency of the reference signal f_{ref}. The digital accumulator is made of an adder (X + Y) and a latch. The output (X + Y) of the adder is latched and then fed to the adder as an input. The other input, X, contains the data to be accumulated. When the total (X + Y) exceeds the maximum size of the adder, an overflow occurs. The division ratio is then changed.

During (K / f_{clock}), the division ratio is set to N + 1, while it is set to N during ($F - K$) / f_{clock}. Therefore, the average division ratio is available after (K / f_{clock}) + (($F - K$) / f_{clock}) = F / f_{clock}. One of the simple fractional-N frequency synthesizers is shown in Figure 33. The overflow of the accumulator directly modulates the division ratio in this figure. The main problem with this implementation is the phase perturbation introduced by the programmable frequency divider. When switching from N to N + 1, the perturbations cause spurious signals at the VCO output. The peak phase deviation at the VCO when changing from N to N + 1 is 2π radians. At the phase detector, it is equivalent to a peak 2π / N. This phase error between the wanted frequency and the instantaneous frequency at the PFD is shown in Figure 34. This phase perturbation is entirely predictable and can be solved by the analog compensation method or the delta-sigma modulation method [19].

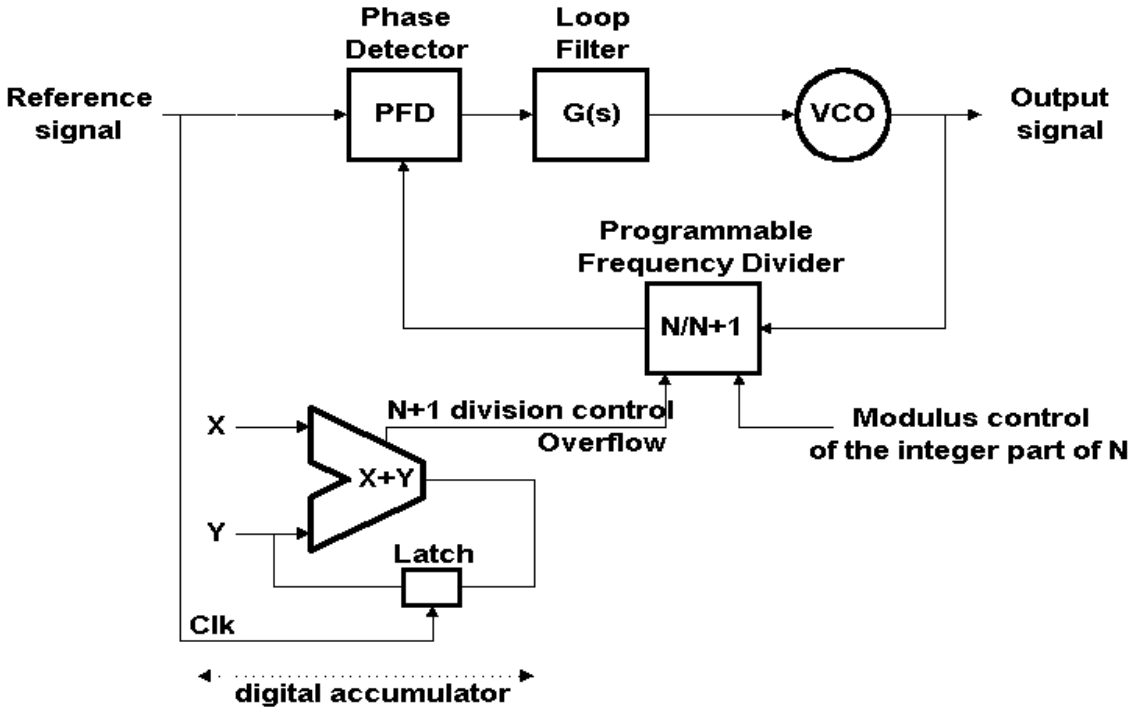


Figure 33. A fractional-N frequency synthesizer

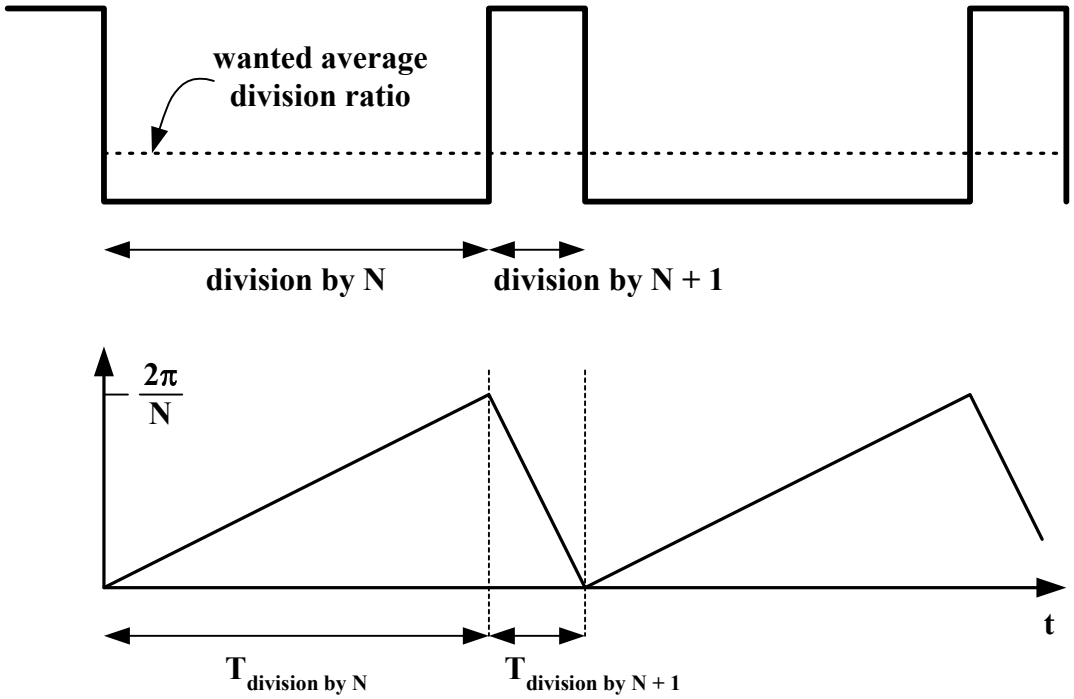


Figure 34. Phase error between the wanted frequency

and the instantaneous frequency at the PFD

In Figure 34, the VCO is too slow at first and then too fast to generate a correct instantaneous frequency. The final phase error over the complete cycle is zero, but a periodic peak occurs in-between for each change in frequency division ratio. If this phase error is not filtered, then it causes severe spurious tones.

The fractional-N frequency synthesizer with analog compensation is presented in Figure 35. The amount of the phase-error accumulation is subtracted from the output of the phase detector. If the two signals match exactly, the analog signal cancels the phase-error signal and reduces the output spurs caused by the fractional synthesis [50]. The precision of the compensation is directly dependent on the Digital-to-Analog Converter (DAC) accuracy and the sensitivity of analog components. On the other hand, the analog

components' characteristics are altered by aging and temperature. Even if the system is well compensated during the early days of design, its property can't last a long time. For that reason, a spurious rejection is limited to 35 ~ 45 dB [17].

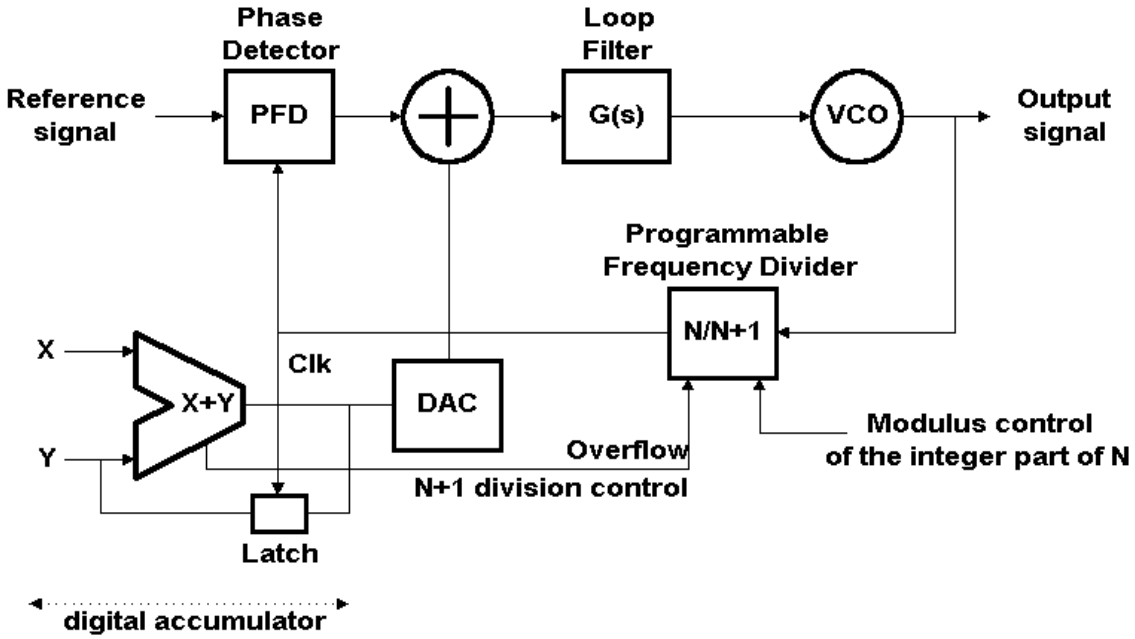


Figure 35. An analog-compensated fractional-N frequency synthesizer

In digital domain, random jittering is used to compensate the phase error generated in loop. The periodic change in the division ratio can be eliminated by injecting a random jitter to the dual-modulus prescaler control block. However, because the injected phase jitter is nearly white noise, this random jittering process generates a relatively high noise floor. It also suffers from a frequency jitter because white noise injected in the frequency domain results in $1/f^2$ noise in the phase domain. Among all the frequency components of white noise, only the low-frequency components of the jitter will pass through the loop and degrade the in-band phase noise in the synthesized signal, since the PLL acts as a low-pass filter for jitter generated by the fractional-N divider.

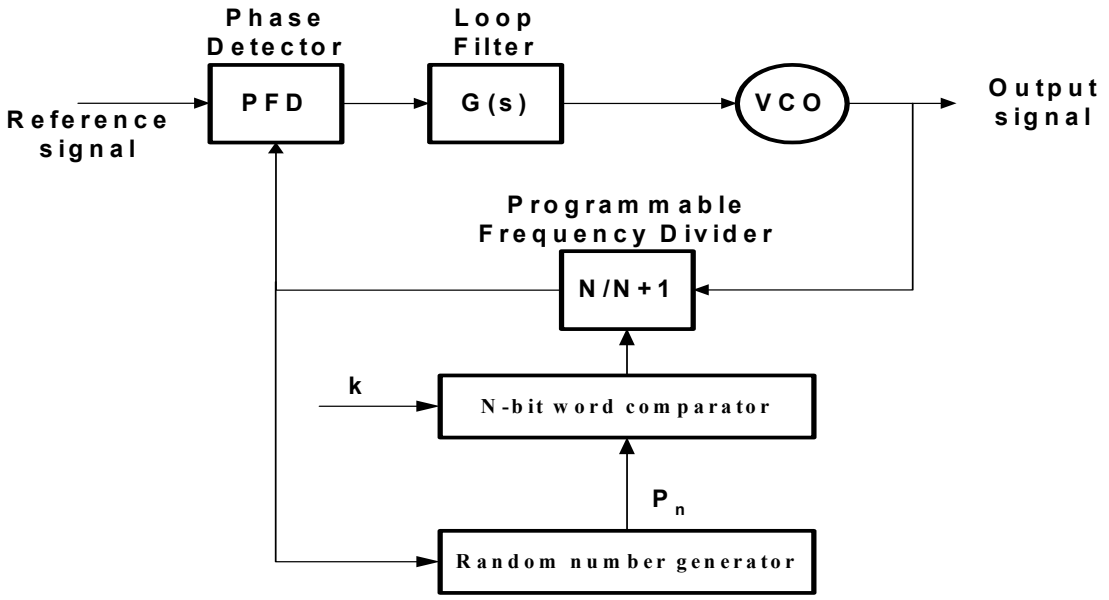


Figure 36. A fractional-N frequency synthesizer with random jittering

The spurs can be eliminated using phase interpolation technique as shown in Figure 37.

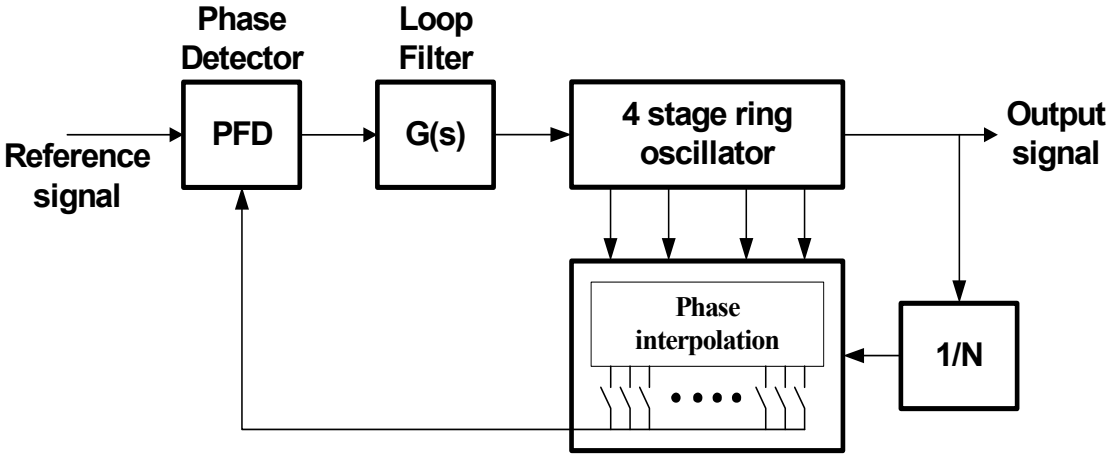


Figure 37. A phase interpolated fractional-N frequency synthesizer

Because an M-stage ring oscillator generates M different phases, these different phases can be utilized to implement a fractional divider using phase interpolation

technique. So, an N.f fractional division can be implemented by the combination of a fixed divider N and phase interpolation from a ring oscillator. In this architecture, a phase interpolator should be used to generate finer phases from the limited phases available in the VCO because the number of inverters in a ring oscillator is limited by the operating frequency. By choosing the correct phase among the interpolated phases, a desired fractional division ratio is generated. This architecture also has several problems that come from the analog imperfections, inaccuracies in the interpolated phase edges generated, and timing uncertainty due to the not-well-defined zero crossing in the phase edges.

Another solution for the perturbation is the delta-sigma modulation method [18]. In Figure 35, a switching of division ratio from N to N + 1 occurs K times over F cycle. This is low frequency switching to reach the wanted phase. If the switching frequency were increased while the ratio of division remains the same during F cycles, the phase noise would be moved to higher frequencies and be filtered by the loop filter. The residual noise remains only at low frequency. Therefore, the overall phase noise of the PLL is reduced. Rather than trying to cancel the phase noise, the system modifies the switching pattern to minimize the low-frequency spectral content caused by the switching of division ratio. The pattern modification can be accomplished by utilizing the noise-shaping technique, which is also called the delta-sigma modulation [19,20,21,22].

In a delta-sigma modulation block, the analog input is fed to an integrator and then passed through a quantizer that works at a high sampling frequency when compared to a Nyquist frequency. A negative feedback loop placed after the quantizer is also added to the input of the integrator. In a frequency-synthesizer application, the input is a digital

word that represents the desired fractional value to synthesize. The first-order delta-sigma modulator is shown in Figure 38.

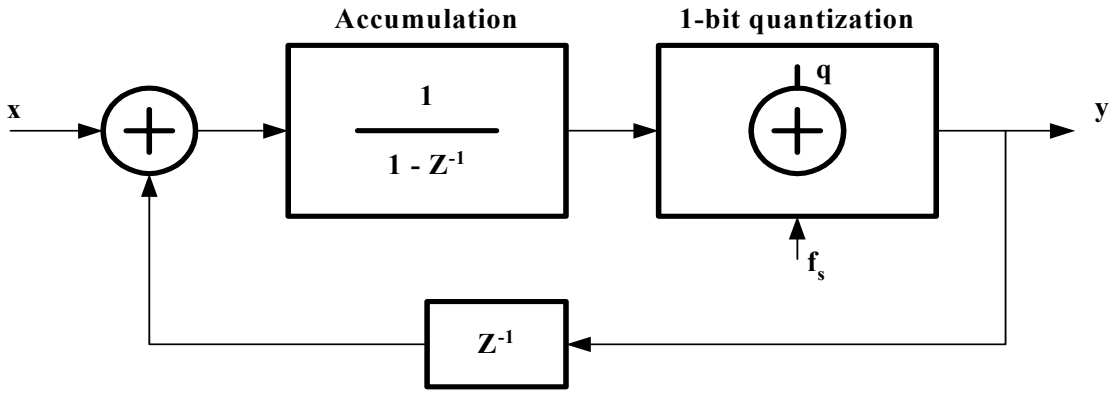


Figure 38. A first-order delta-sigma modulator

In Figure 38, the transfer function of the integrator H_{int} is expressed by

$$H_{int} = \frac{1}{(1 - z^{-1})} \qquad \text{(eq. 59)}$$

Then, the expression for the output of the first-order delta-sigma modulator y is given by

$$y(z) = \left(\frac{H_{int}}{(1 + z^{-1} H_{int})}\right) x(z) + \left(\frac{1}{(1 + z^{-1} H_{int})}\right) q(z) \qquad \text{(eq. 60)}$$

$$= x(z) + (1 - z^{-1})\, q(z) \qquad \text{(eq. 61)}$$

$$= x(z) + H_{noise}(z)\, q(z) \qquad \text{(eq. 62)}$$

where q(z) is the quantization noise and x(z) is the input signal

The H_{noise} portion has a high-pass filtering property. Therefore, the input signal is transferred, but the quantization noise is high-pass filtered by the delta-sigma modulator [15]. Thus, if the delta-sigma modulator block is followed by a low-pass filter, then the high-frequency component H_{noise} is filtered out and only the signal component x(z) remains. In reality, a first-order delta-sigma modulator is not sufficient for suppressing

the phase-noise in a frequency synthesizer application; therefore, a third or fifth order is commonly used. The equation for a third-order structure is given by

$$y(z) = A + B\cdot(1 - z^{-1}) + C\cdot(1 - z^{-1})^2 \quad \text{(eq. 63)}$$

$$= x(z) + q_1(z)\cdot(1 - z^{-1}) + (-q_1(z) + q_2(z)\cdot(1 - z^{-1}))\cdot(1 - z^{-1})$$

$$+ (-q_2(z) + q_3(z)\cdot(1 - z^{-1}))\cdot(1 - z^{-1})^2 \quad \text{(eq. 64)}$$

$$= x(z) + (1 - z^{-1})^3\, q_3(z) \quad \text{(eq. 65)}$$

$$= x(z) + H_{noise}(z)\, q_3(z) \quad \text{(eq. 66)}$$

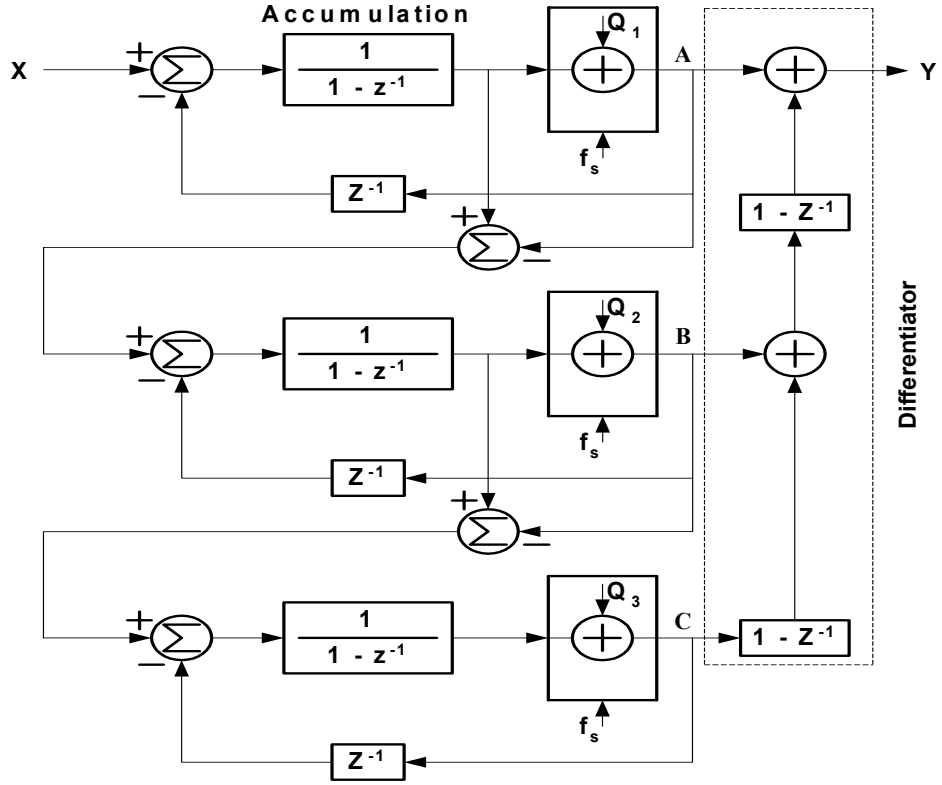


Figure 39. A third-order MASH

A phase noise introduced by the division-ratio switching using third-order Multi-stAge noise SHaping (MASH) can be obtained from the equation (66), $f_{vco} = (N_{integer} + N$

$_{fractional}$) $f_{ref} = N f_{ref} + ((K / F) + H_{noise}(f) q_3(f)) f_{ref}$. If the quantization noise q is uniformly distributed, then the phase noise is given by

$$S_\phi(f) \approx \frac{(2\pi)^2 \left(\frac{2\pi f}{f_{ref}}\right)^{2(n-1)}}{(12\ f_{ref})} \qquad \text{(eq. 67)}$$

Therefore, if MASH controls the fractional-frequency division ratio, the quantization noise moves to a higher frequency and is shaped as shown in equation (67). Then, higher frequency components are removed by the low-pass characteristic of PLL. Thus, the spurious noise level is reduced. The third-order MASH structure is shown in Figure 39 and a frequency synthesizer using third-order MASH is shown in Figure 40.

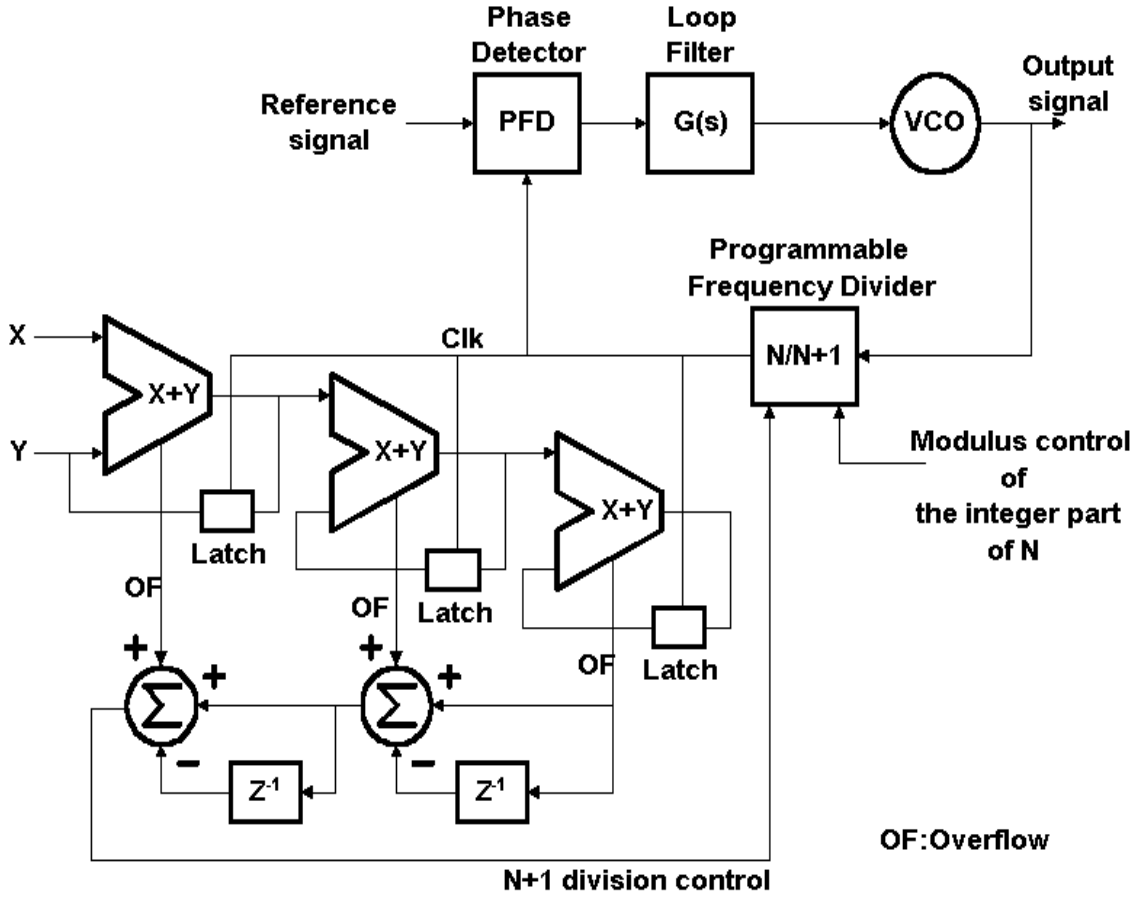


Figure 40. A frequency synthesizer using third-order MASH

3.3 All-Digital Frequency Synthesizer (ADFS)

As described in previous sections, most blocks of PLL-based frequency synthesizers are comprised of digital circuits. However, some blocks consist of analog circuits such as a charge-pump or a continuous-time analog filter. Therefore, most PLL-based frequency synthesizers are not fully digital systems. Furthermore, all continuous-time analog filters are made of external passive-components. So, the characteristics of such analog blocks vary because of variations in the passive elements' values. Even worse, the center frequency of a frequency synthesizer is influenced by parasitic capacitors on the frequency synthesizer chip. The resulting variations can be so big that trimming may become necessary in critical applications. Many parameters are also subject to change in case of temperature drifts. The problem can be reduced using the All-Digital Frequency Synthesizer (ADFS). In contrast to conventional Digital Phase-Locked Loop (DPLL), it is an entirely digital system. To realize an ADFS, all function blocks of the system must be implemented using purely digital circuits. One of the digital versions of the phase detector is a flipflop-counter phase detector and a loop filter can be replaced with an up/down counter. The digital counterpart of the VCO is the Digital-Controlled Oscillator (DCO) such as ÷N counter DCO, which is used to scale down the signal generated by a high-frequency oscillator that operates at a fixed frequency [46]. The details of phase detectors, loop filters and VCOs will be discussed in later sections of this chapter. In general, settling time of the ADFS methods can be made extremely short. Such short settling time can be an advantage in some applications; however, there are other instances where a slower response combined with a better noise-suppression capability is preferred. Because a trade-off always exists between frequency

step-size and settling time, not all RF specifications are easily met using the ADFS methods.

The EXOR gate, edge-triggered JK-flipflop, and PFD can also be used as a phase detector in all-digital frequency synthesizer. The operations and transfer characteristics of these three phase detectors are shown in Figure 41 [52].

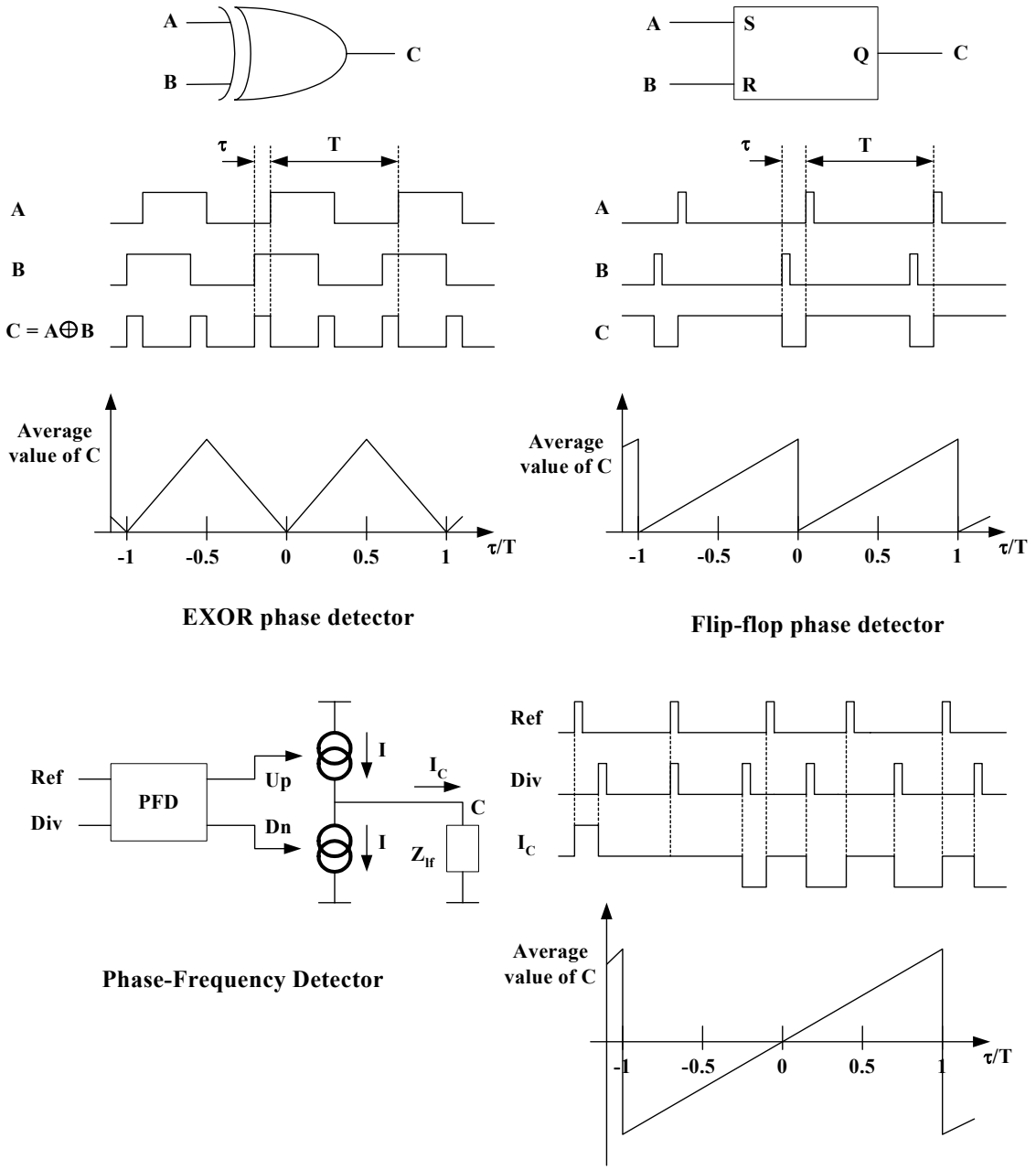


Figure 41. The operations and transfer characteristics of phase detectors

The output waveform of an EXOR phase detector has an average value that is proportional to the phase difference over a range of half a cycle as indicated in Figure 41. The output C does not contain any energy at the reference frequency, but the second harmonic reaches maximum amplitude of 1.27 times the peak-to-peak range of the PD characteristic at a phase difference of 90°. Unfortunately, this is exactly the operating point that will be chosen as the center of operation, as it is situated at the middle of the linear range. In a flipflop phase detector, narrow pulses at both input A and B set and reset the output C. The average value of C has the shape of a saw-tooth, with a linear range of a full cycle. In the middle of this linear range, the output has a component at the reference frequency with a magnitude of 1.27 times the peak-to-peak range of the PD. The PFD is also a sequential PD like the EXOR and flipflop phase detector but contains a memory function that allows it to give some information about the frequency when the loop is not in a locked status. The operation principle of the PFD is also shown in Figure 41. The reference pulse causes the output to change in a positive direction, unless the output is already positive, in which case the pulse has no effect. Similarly, the loop's divider output causes a negative transition unless the output is already negative. The linear phase range is 720°. At a locked position, the output contains no spurious signals at all because the up- or the down-pulse does not occur. However, the PFD has crossover distortion, changes in gain that occur near zero phase error [46,59].

A logical evolution of the simple flipflop PD is the flipflop-counter phase detector shown in Figure 42. In this PD, the reference input and output signals of the VCO are binary valued. These signals are used to set or reset an edge-triggered RS flipflop. The time period in which the Q output of the flipflop is logic '1' is proportional to the phase

error θ_e. The Q signal is used to gate the high-frequency clock signal into the counter. Note that the counter is reset on every positive edge of the reference signal. The content N of the counter is also proportional to the phase error θ_e, where N is the n-bit output of this type of phase detector. Sometimes, the Nyquist-rate phase detector, Hilbert-transform PD, and zero-crossing PD can be used as a PD in an all-digital frequency synthesizer.

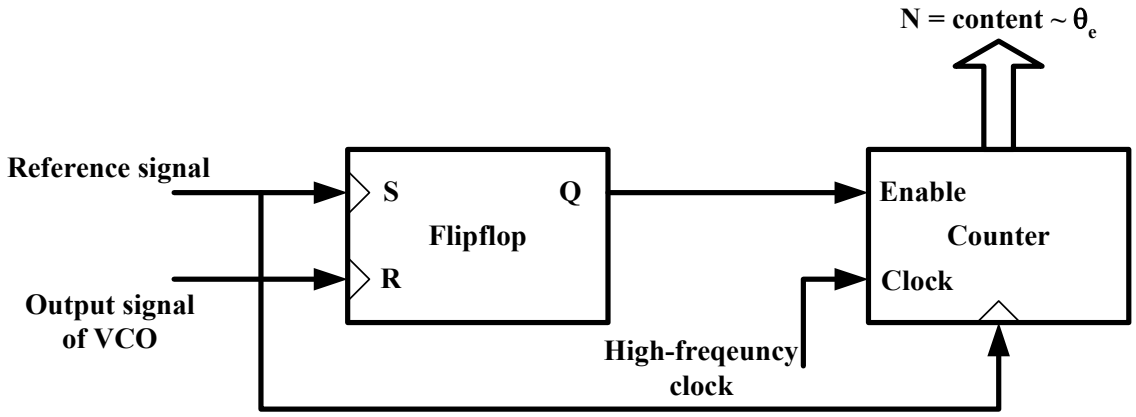


Figure 42. A flipflop-counter PD

The simplest loop filter is built from an ordinary Up/Down counter. The preferable Up/Down counter loop filter operates in combination with a phase detector delivering Up or Dn pulses, such as the PFD. It is easily adapted, however, to operate in conjunction with the XOR or JK-flipflop phase detectors and other types of PDs. As shown in Figure 43, a pulse-forming network is first needed which converts the incoming Up and Dn pulses into a counting clock and a direction ($\overline{\text{Up/Dn}}$) signal. On each Up pulse generated by the phase detector, the content N of the Up/Dn counter is incremented by 1. A Dn pulse will decrease N in the same manner. The content N is given by the n-bit parallel output signal of the loop filter. Because the content N is the weighted sum of

the Up and Dn pulses, this filter can roughly be considered as an integrator having the transfer function

$$H(s) = \frac{1}{s \cdot T_i} \qquad \text{(eq. 68)}$$

where T_i is the integrator time constant.

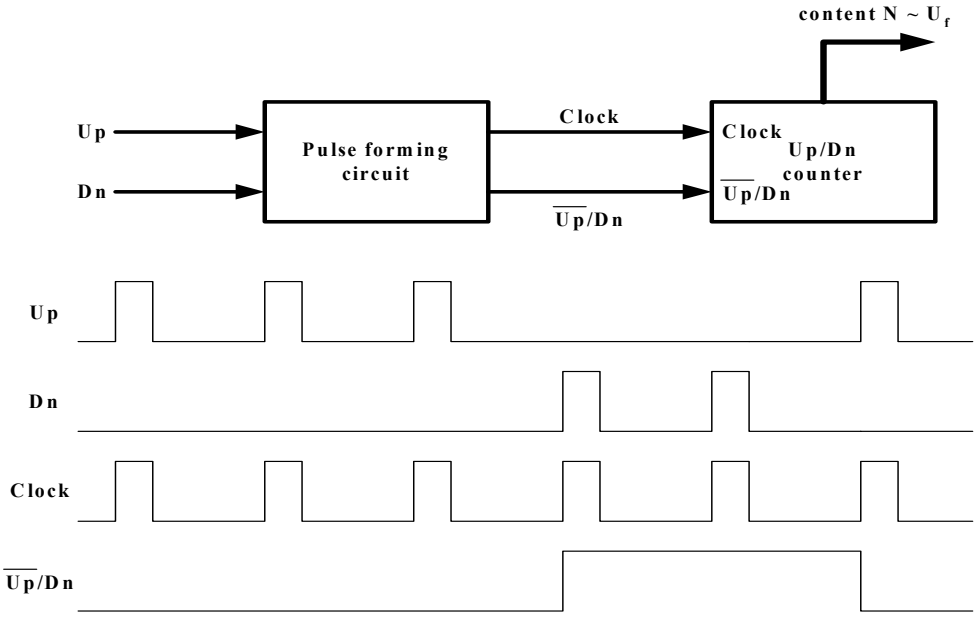


Figure 43. An Up/Dn counter loop filter

One of the most important digital loop-filter that works with the EXOR or the JK-flipflop phase detector is the K counter which is composed of two independent counters, referred to as "Up counter" and "Down counter." K is the modulus of both counters; i.e., the contents of both counters is in a range from 0 ~ (K – 1). K can be controlled by the K modulus control input and is always an integer of power of two [58]. The frequency of the clock signal is M times the center frequency f_0 of the ADFS, where M is typically 8, 16, 32, and so on. The operation of the K counter is controlled by the Dn/Up signal. If this signal is high, the "Down counter" is active, while the contents of the Up counter of

the Up counter stays frozen. In the opposite case, the "Up counter" counts up but the Down counter stays frozen. Both counters recycle to 0 when the content exceeds K – 1. The most significant bit of the "Up counter" is used as a "carry" output, and the most significant bit of the "Down counter" is used as a "borrow" output. Consequently, the carry is high when the content of the Up counter is equal to or more than K/2. In analogy, the borrow output gets high when the contents of the Down counter is equal to or more than K/2. The positive-going edges of the carry and borrow signals are used to control the frequency of a digitally controlled oscillator.

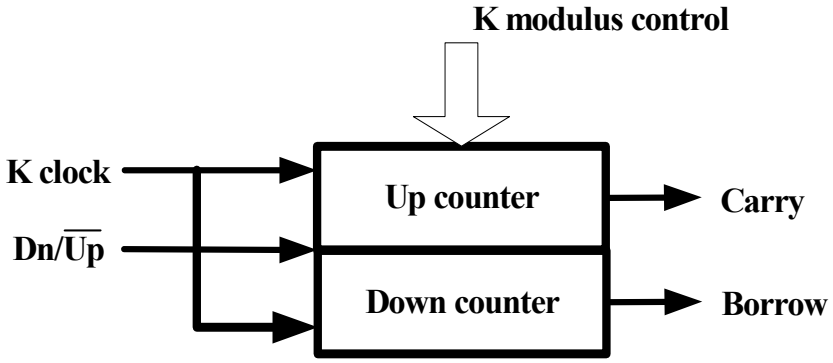


Figure 44. A K counter loop filter

A variety of Digital-Controlled Oscillators (DCOs) can be designed by hardware or by software. The ÷N counter DCO and Increment-Decrement (ID) counter are the most popular DCO that is implemented by hardware. However, the waveform synthesizer DCO lends itself almost ideally to implementation by software. In general, the output frequency of these DCOs cannot be as high as the frequency of their clock, but at most two-thirds of that value. Therefore, this limits the hold range of the ADFS [46].

3.4 Conclusion

This chapter has given an overview of the frequency synthesizer techniques and their performance criteria. Specifically, low phase noise, low spurious tone, low-power single chip solution for wireless communication is the main focus of this chapter.

The direct synthesizer is a straightforward way to implement a frequency synthesizer. Using this frequency synthesizer, an accurate frequency is attainable by repeatedly mixing and dividing. Ideally, the output spectrum is as clean as the reference spectrum and a fast frequency hopping is possible. However, when implementing the direct synthesizer, cross-coupling between stages is a serious problem for the spectral purity and the large number of components causes the synthesizer to be very bulky and power hungry. Another obvious drawback associated with the direct synthesizer is high costs.

A table-look-up technique has attractive features such as fast locking speed, high integration level, and wide tuning range. On the other hand, this architecture has several disadvantages such as high power consumption, limitation of higher frequency by Nyquist theorem, and discrete narrow band spurs. So, a table-look-up synthesizer is usually combined with a fixed-frequency Phase-Locked Loop (PLL) frequency synthesizer to overcome its highest-frequency limitation [10]. This combined synthesizer is called a Direct Digital Frequency Synthesizer (DDFS). This architecture also has disadvantages such as the limited frequency range because of the low F_{low}, which can only be increased by making a faster DAC. Therefore, the DDFS will only be useful in systems that require very fast frequency hopping.

The phase-locked loop based frequency synthesizer has many advantages such as the potential for combining high frequency and low power, low cost, effective spurious-noise suppression and its easiness of integration in low-cost IC processes, like CMOS. This is the reason why the PLL is most popular in almost all wireless communication chip sets on the market [11]. However, this architecture has many major disadvantages such as the inverse relationship between the step size and the phase noise. As the step size decreases, division ratios in the system must increase. The higher the division ratio, the worse the phase noise within the loop bandwidth close to the center frequency. Another drawback is a slow switching speed from one frequency to another because of the negative-feedback loop dynamics.

A dual- or multi-loop frequency synthesizer is one of the recently developed methods. In this method, a mixer is incorporated into the PLL. The method can alter the relationship between the channel spacing and the reference frequency of integer-N synthesizers by employing two or more loops. So, using this architecture, the loop bandwidth can be large. However, the dual-loop frequency synthesizer has the sidebands produced from non-ideal SSB mixing and consumes more power than the single-loop method [12].

Another way to implement a frequency synthesizer is the fractional-N method [13,14,15]. The fractional-N frequency synthesizer does not require additional currents, circuit complexity, or larger dies than the other methods. However, using the fractional-N frequency synthesizer, the phase noise is theoretically improved by $20 \cdot \log (F)$. The main problem with this implementation is the phase perturbation introduced by the programmable frequency divider. When switching from N to N + 1, the perturbations

cause spurious signals at the VCO. The most popular technique for solving this perturbation is the delta-sigma modulation method [18]. If the divider switching frequency were increased while the ratio of division remains the same during F cycles, the phase noise would be moved to higher frequencies and be filtered by the loop filter. The residual noise remains only at low frequency. Therefore, the overall phase noise of the PLL is reduced. Rather than trying to cancel the phase noise, the system modifies the switching pattern to minimize the low-frequency spectral content caused by the switching of division ratio. The pattern modification can be accomplished by utilizing the noise-shaping technique, which is also called the delta-sigma modulation [19,20,21,22].

The problems that are caused by analog circuits such as variation in the passive elements' values or shift of the center frequency of a frequency synthesizer can be solved using the All-Digital Frequency Synthesizer (ADFS). In contrast to conventional Digital Phase-Locked Loop (DPLL), it is an entirely digital system. So, settling time of the ADFS methods can be made extremely short. Such short settling time can be an advantage in some applications; however, there are other instances where a slower response combined with a better noise-suppression capability is preferred. Because there is always a trade-off between frequency step-size and settling time, not all RF specifications are easily met using the ADFS methods.

Chapter 4

Design of Frequency Synthesizer

As described in the previous chapter, the All-Digital Frequency Synthesizer (ADFS) can be used to reduce the number of required external passive-components and to reduce the variation of its characteristics by its parasitic or temperature drifts. Additionally, the settling time of ADFS methods can be made extremely short and variable. Such short and variable settling time can be an advantage in some applications such as multi-mode, multi-application.

Using the basic concept of ADFS, a fully integrated, fast-locking fractional-N frequency synthesizer has been designed. In this design architecture, large and inaccurate capacitors and resistors in a loop filter are substituted by a programmable digital Finite Impulse-Response (FIR) filter to remove the analog continuous-time loop filter whose performance is sensitive to process and temperature variations and aging. Second, the adaptive loop-gain control proportional to the frequency difference was used to make frequency locking time fast. Lastly, the phase noise and spurs have been reduced by a Multi-stAge Noise SHaping (MASH) controlled Fractional Frequency Detector (FFD) that generates a digital output corresponding directly to the frequency difference. So, the frequency synthesizer designed for this thesis offers a high integration ability, technology robustness, fast locking time, low noise level, and multi-mode flexibility.

To prove performance of the newly designed frequency synthesizer, a Bluetooth application frequency synthesizer system was implemented using 0.18 um CMOS

technology. Analysis, design, and simulation were carried out at both the system and the circuit levels. Then, the performance was also verified by fabrication.

4.1 System Consideration

The topology of the designed frequency synthesizer is shown in Figure 45. It is composed of a Fractional Frequency Detector (FFD), reference divider, amplitude detector, variable gain block, accumulator, FIR digital filter, Digital-to-Analog Converter (DAC), VCO, prescaler, and third-order MASH engine. In this architecture, the FFD serves as a frequency-difference gauge between the $f_{reference}$ and the $f_{feedback}$, and outputs a digital value that is directly proportional to the frequency difference. Then, the output is fed into the variable gain block, whose gain is proportionally controlled by the amplitude of the FFD output. Because of this adaptive gain control, the acquisition time is reduced; however, the system performance after the locking is not affected by the acquisition mode characteristics. The signal multiplied by a gain is low-pass filtered by an accumulator. Then, the filtered data is divided into two parts: the Most Significant Bit (MSB) bits part that controls the switches of the switched-current VCO and the Least Significant Bit (LSB) bits part that is followed by a FIR digital filter and a DAC. The LSB bits part controls the tuning voltage of a Voltage Controlled Resistor (VCR).

The MSBs and the LSBs then decide together the coarse and fine frequency ranges of the VCO output by controlling the switches that adjust the amount of the tail current and the tuning voltage of a VCR. After that, the output signal of the VCO, f_{out}, is divided by the prescaler because developing a FFD that operates reliably at 2.4 GHz or higher is rather difficult. Next, the divided data frequency, $f_{feedback}$, is compared with the

reference frequency. Through these procedures, the frequency acquisition is completed. After the frequency locking, the phase acquisition is performed to lock the phase by resetting the VCO.

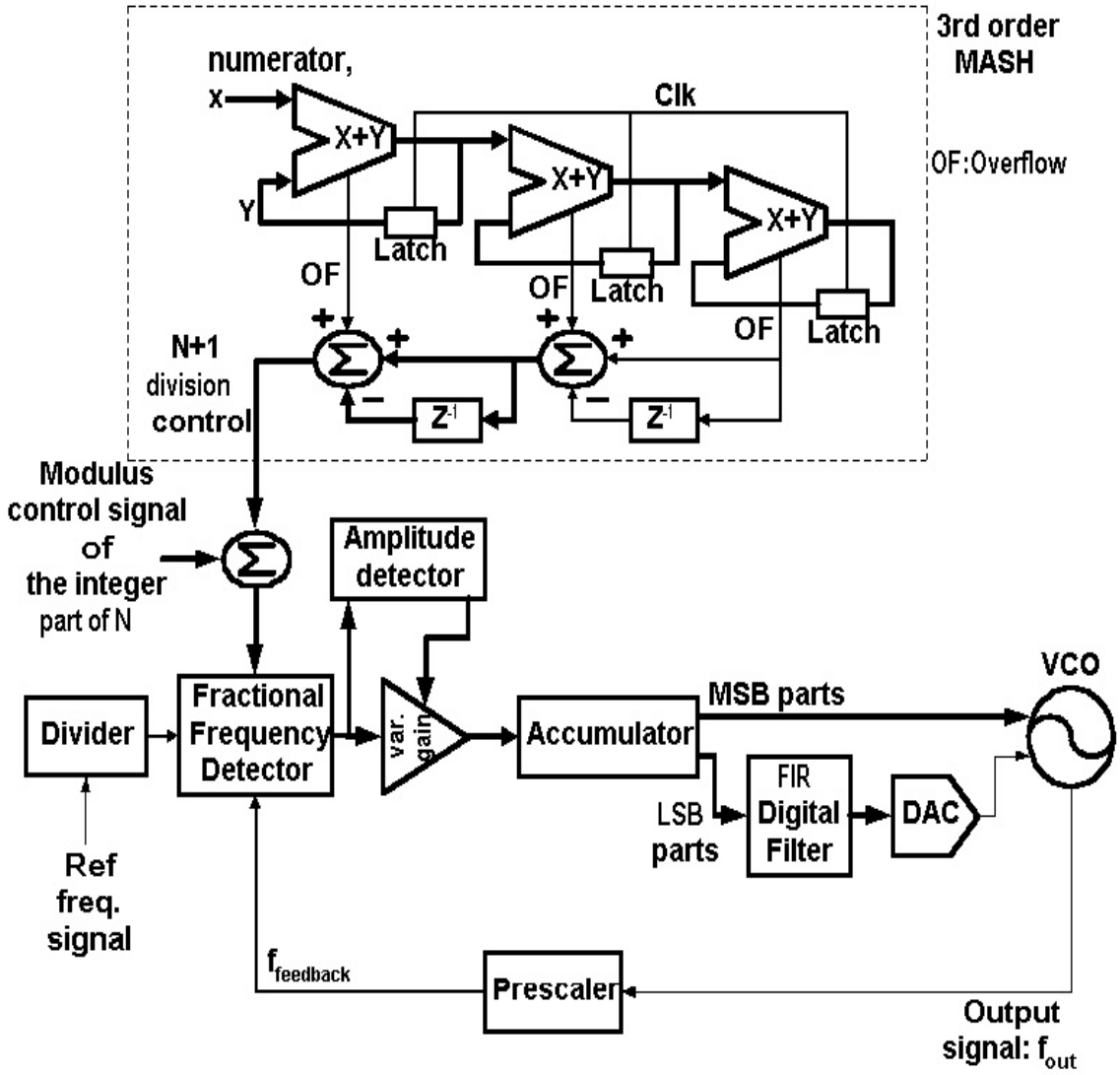


Figure 45. The architecture of the proposed frequency synthesizer

A third order MASH engine and a FIR digital filter were used in the designed architecture to produce fractional output frequency. The FFD, which is made up of a down counter and a sampler that counts the $f_{feedback}$ clock pulse downward during the

reference period. Thus, the modulus control value N is set by the initial value of the down counter. The fractional effect can be obtained by adding the output value of a third-order MASH engine and the modulus control value N. However, this change of modulus results in a rapid variation of the accumulator LSB bits part value. Thus, filtering is needed to remove high-frequency elements. The filtering function is performed by FIR digital filter. After the filtering, the data is converted to an analog signal and used as the tuning voltage for the VCR.

4.2 System Simulation Results

Although the designed frequency synthesizer is a non-linear device because many non-linear devices are in the system, it can be accurately modeled as a linear device when the loop is in a locked mode. Figure 46 shows the linear model of the designed frequency synthesizer when it's in a locked mode. In this figure, the accumulator is replaced by the equation, $1/(1-z^{-1})$, and the F(z) is the FIR digital function.

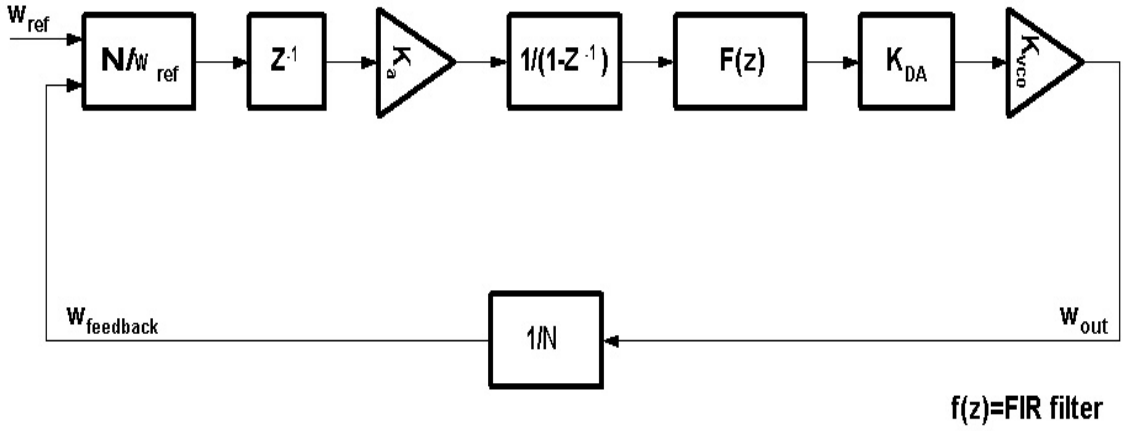


Figure 46. Linear model of the proposed frequency synthesizer

Based on the above figure, the closed-loop gain of the designed frequency synthesizer is given by

$$H(z) = \frac{\omega_{feedback}}{\omega_{ref}} = \frac{K \cdot F(z) \cdot z^{-1}}{1 - z^{-1}\left(1 - K \cdot F(z)\right)} \qquad \text{(eq. 69)}$$

$$\text{where, } K = \frac{K_{DA} \cdot K_{VCO} \cdot K_a}{\omega_{ref}}$$

In this equation, the system stability is not related directly to the order of digital FIR filter, F(z), but the K has to be approximately smaller than 0.9 for stability. To check the frequency acquisition time and its stability, the unit step response and the pole-zero plot are shown in Figure 47 and Figure 48. In Figure 47, the time required for $\omega_{feedback}$ to reach the final value is within 220 times of (1 / reference frequency), which is less than the Bluetooth specification. This required time could be reduced by enlarging the value of K. As shown in Figure 48, all the poles are inside the unit circle in z-domain.

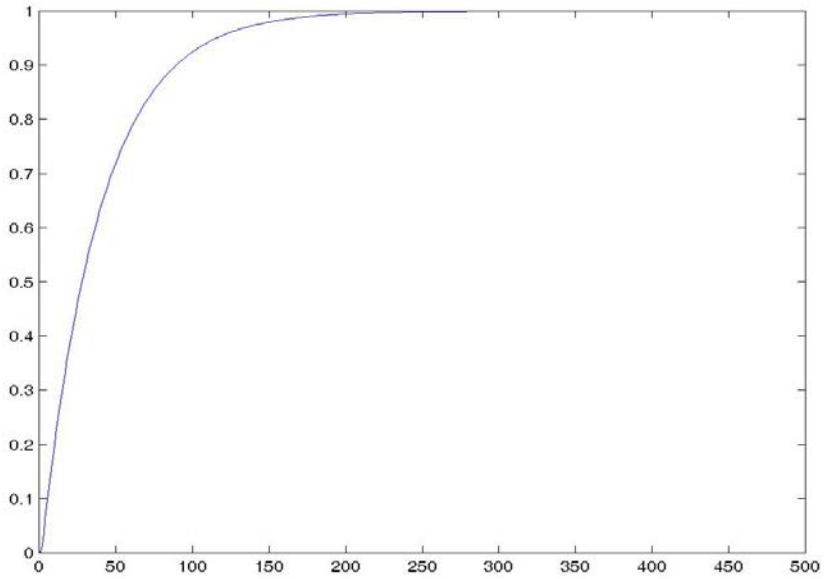


Figure 47. The unit step response

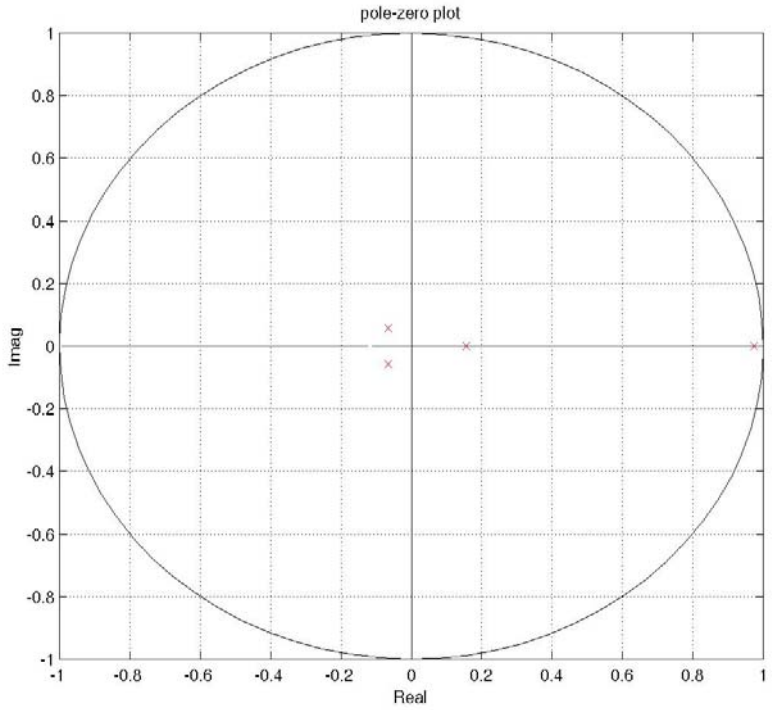


Figure 48. The pole-zero plot when fourth-order FIR filter is used

To verify the switching speed of the designed frequency synthesizer at its system level, worst-case time domain simulations have been carried out using Matlab® simulator when the output signal is changed from bottom limit to upper limit of the Bluetooth frequency range. The worst-case simulation results are shown in Figure 49. At the reference frequency of 1 MHz, the output of the designed frequency synthesizer settles down within 220 usec. Under same system-level simulation condition, the settling time of the classical charge-pump frequency synthesizer is approximately 300 usec. Therefore, the newly designed frequency synthesizer has a faster switching speed at the system level than the classical frequency synthesizer. The designed frequency synthesizer meets the Bluetooth application settling specification at the system level.

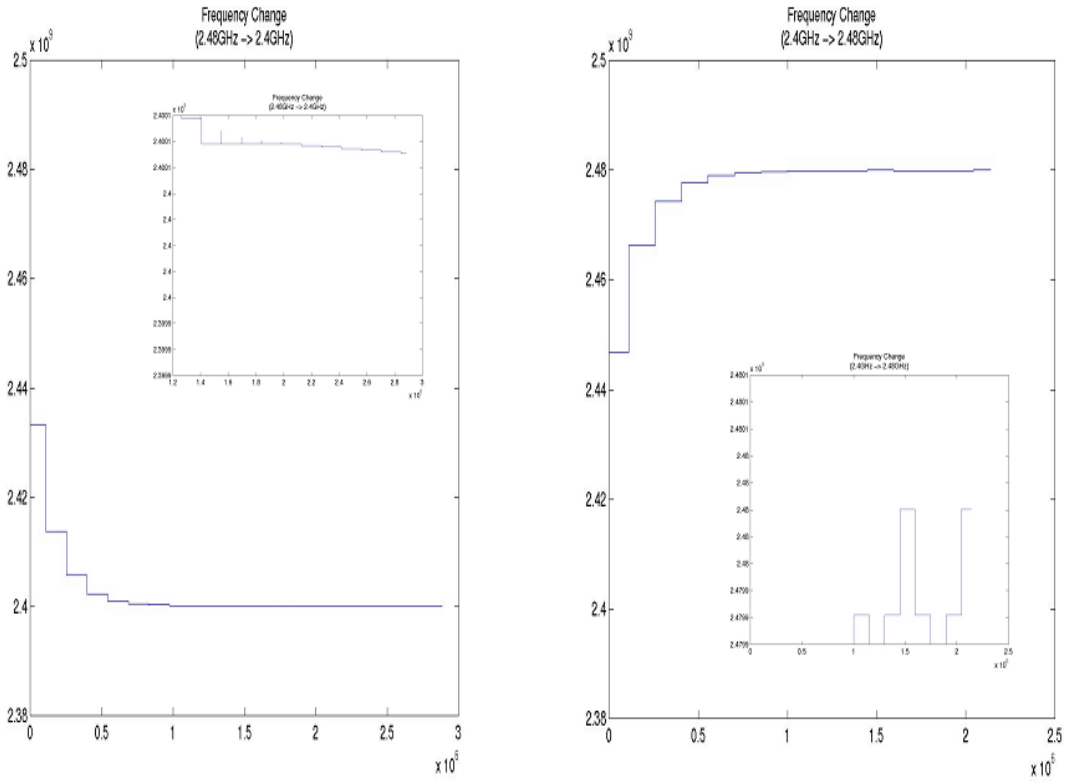


Figure 49. The worst-case time domain simulation of the proposed frequency synthesizer

The primary purpose of frequency synthesizer is to provide programmable, clean signals to generate clock signals or local oscillator signals. Therefore, phase noise is the most important specification for a frequency synthesizer. Generally, the loop filter is designed only to guarantee the stability of the closed-loop system. The phase-noise optimization procedure is run on a trial-and-error basis. A typical practice is to design the loop filter to stabilize the system. Then, simulation programs such as SpectraRF, HP-ADS and MDS are used to improve the phase-noise performance by adjusting the loop-filter parameters. Because the total noise-power-spectrum density at the VCO output is related to the noise sources and the loop-filter parameters, each building block is designed and loop-filter parameters are chosen with the objective of minimizing the noise

sources. The Bluetooth phase-noise specifications are given as –89 dBc/Hz at 500 KHz offset frequency and -121 dBc/Hz at 2 MHz offset frequency. The system-level simulation results of phase noise and spurs are shown in Figure 50.

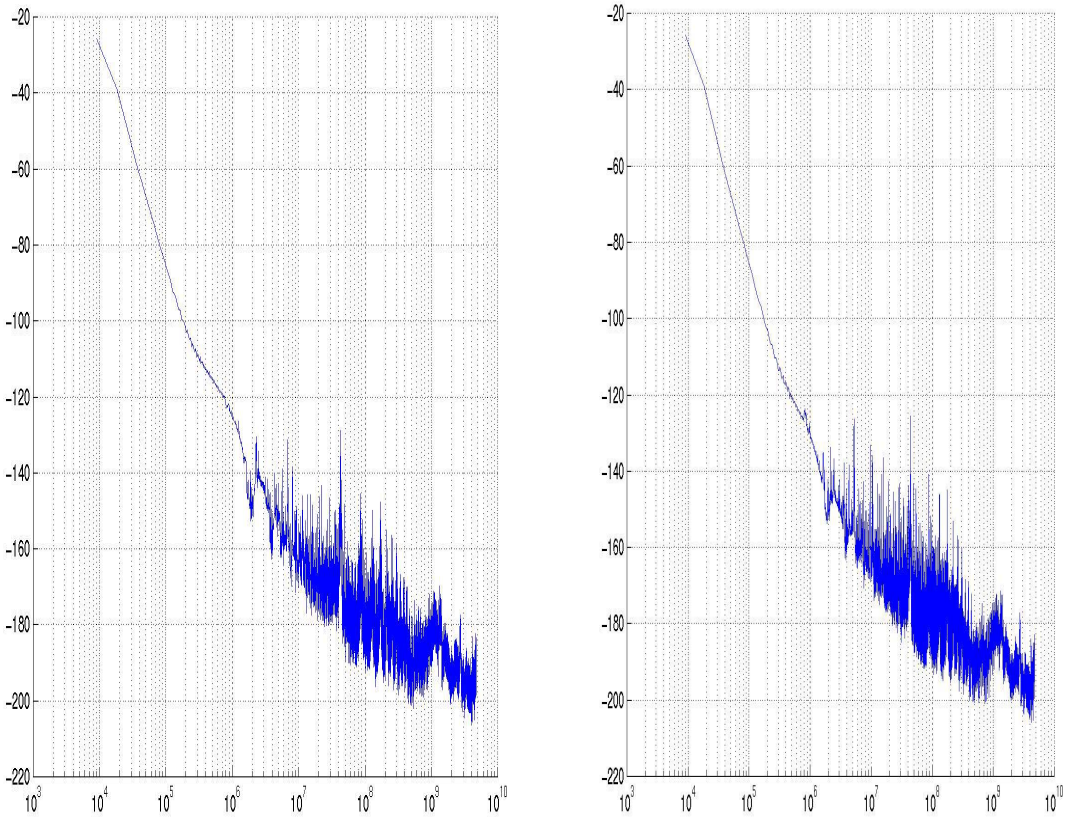


Figure 50. A phase noise and spurs of the proposed frequency synthesizer

(a) Fractional factor = 32 /65 (b) Fractional factor = 0 /65

4.3 Implementation of Key Building Blocks

The designed frequency synthesizer has been implemented using 0.18 um CMOS technology of National Semiconductor. In this section, the details of the critical functional blocks that compose the designed frequency synthesizer will be explained.

4.3.1 Fractional Frequency Detector (FDD)

As explained in the previous section, the Fractional Frequency Detector (FFD) measures the frequency difference between the reference frequency and the VCO output frequency by counting the VCO output signal during a period of reference frequency. The FFD is made up of a sampler that is used in sampling the VCO output signal and the eight-bit up/down counter. Using the initial value setting of this eight-bit up/down counter, the application of this frequency synthesizer can be changeable even if the division ratio range of divider is small or fixed.

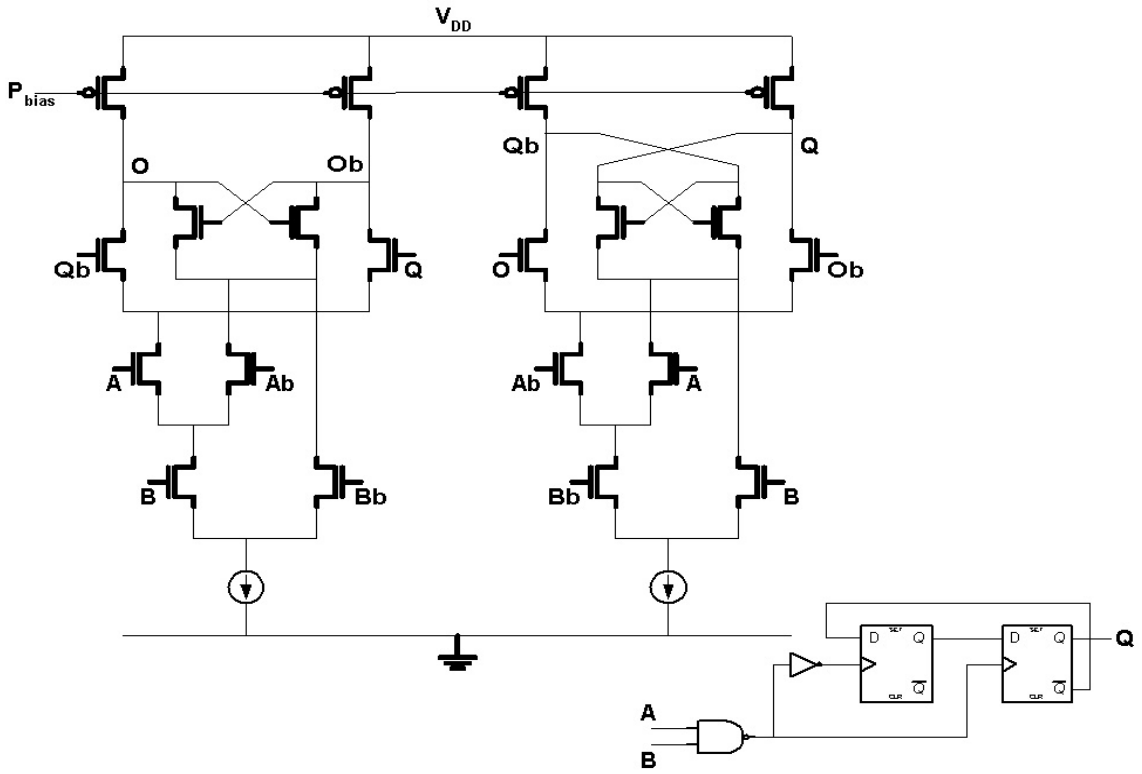


Figure 51. The part of up/down counter

The up/down counter is designed using Current Mode Logic (CML) that is shown in Figure 51. In a conventional logic design, CMOS static logic is most commonly used

for its wide noise margins, high packaging density, and zero static-power dissipation. However, if many gates operate at high switching speed, the large dynamic current pulses flow through the parasitic capacitance, resistance, and inductance associated with power-supply lines and a substrate. These current pulses result in couplings between the analog blocks and the digital blocks, which in turn increases the phase noise of the VCO. Additionally, the CMOS static logic's single-ended circuit is susceptible to power-supply noise. The noises can be reduced by the CML that uses constant current source and has differential input and output signals. Using the CML, the digital noise is reduced because of its constant current source, and the noise from the power line and substrate is reduced because of its differential structure [23,25].

Figure 51 shows a part of up/down counter that uses CML. This figure includes two latches, one NAND, and one inverter that are used to implement an up/down counter. Because a NAND and an inverter are embedded with latches in critical path, the maximum input frequency at a given power is increased. Figure 52 shows the SpectraRF simulated waveforms of the designed FFD. In this simulation, the initial value of the up/down counter in FFD is set to '0001 0111 1111' to implement the Bluetooth standard and the input reference signal is 1 MHz. If the output signal from the VCO is fed to FFD, then the up/down counter starts to count down by the end of input reference signal. So, the residual value of the up/down counter represents the difference between input reference signal and VCO output signal. In this architecture, the multi-mode or multi-application can be implemented only by changing the initial value of the up/down counter in FFD with a loop filter that has variable cut off frequency such as programmable finite impulse response digital filter.

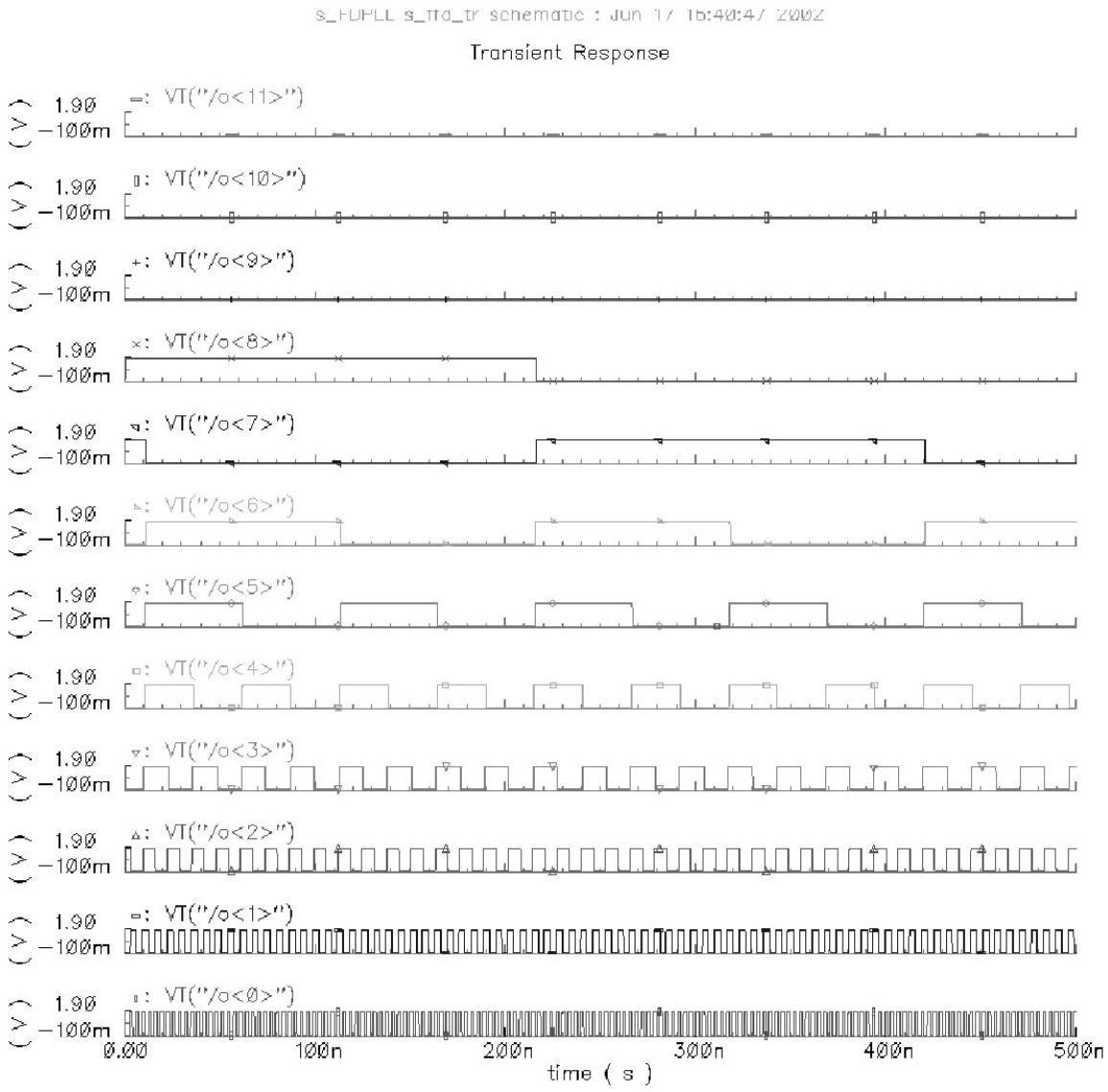
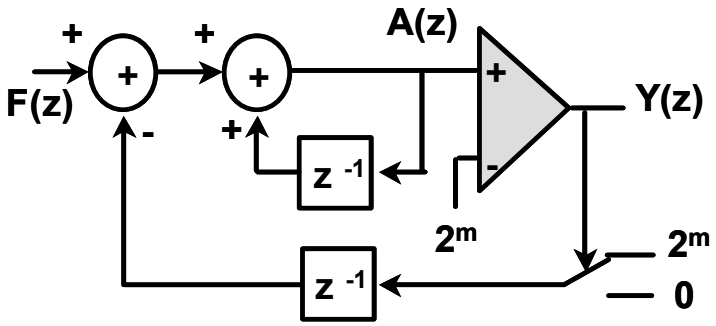


Figure 52. A simulation result of designed FFD

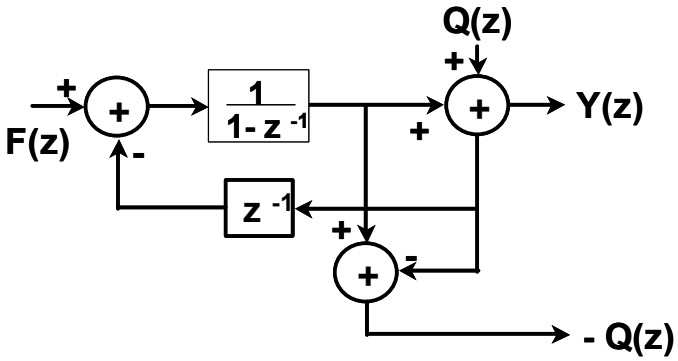
4.3.2 Third-order MASH

As discussed in earlier chapter, in a delta-sigma modulation block, the digital word that represents the desired fractional value is fed to an integrator and then passed through a quantizer that works at a high sampling frequency when compared to a Nyquist frequency. A negative feedback loop placed after the quantizer is also added to the input

of the integrator. The first-order delta-sigma modulator is shown in Figure 38 and its discrete sigma-delta modulator that is implemented by replacing the analog blocks with an m-bit accumulator, a latch, and an adder is shown in Figure 53 [19,45,54].



(a)



(b)

Figure 53. A first-order delta-sigma modulator

(a) a model of the accumulator (b) a modulator's z domain model

A modulated fractional division value generator that is made by third-order MASH based on cascading first-order delta-sigma modulator is shown in Figure 54. In this generator, the division ratio increases by one if an overflow is encountered. The division ratio decreases by one after a one-cycle delay. This increases the divide-ratio changing frequency while keeping the average division ratio the same, thus pushing away

the spurs from the center frequency of VCO. The modulated fractional division value generator consists of three accumulators, latches, and adders. An m-bit accumulator is made up of an m-bit adder and m-bit latches. The six-bit Manchester adder is used as an adder in an accumulator. This adder uses a three-input multiplex to improve its speed. In this adder, the i-th carry, C_i is given by

$$C_i = G_iP_i + P_iC_{i-1} \qquad \text{where, } G_i = A_i \cdot B_i \text{ and } P_i = A_i \oplus B_i \qquad \text{(eq. 70)}$$

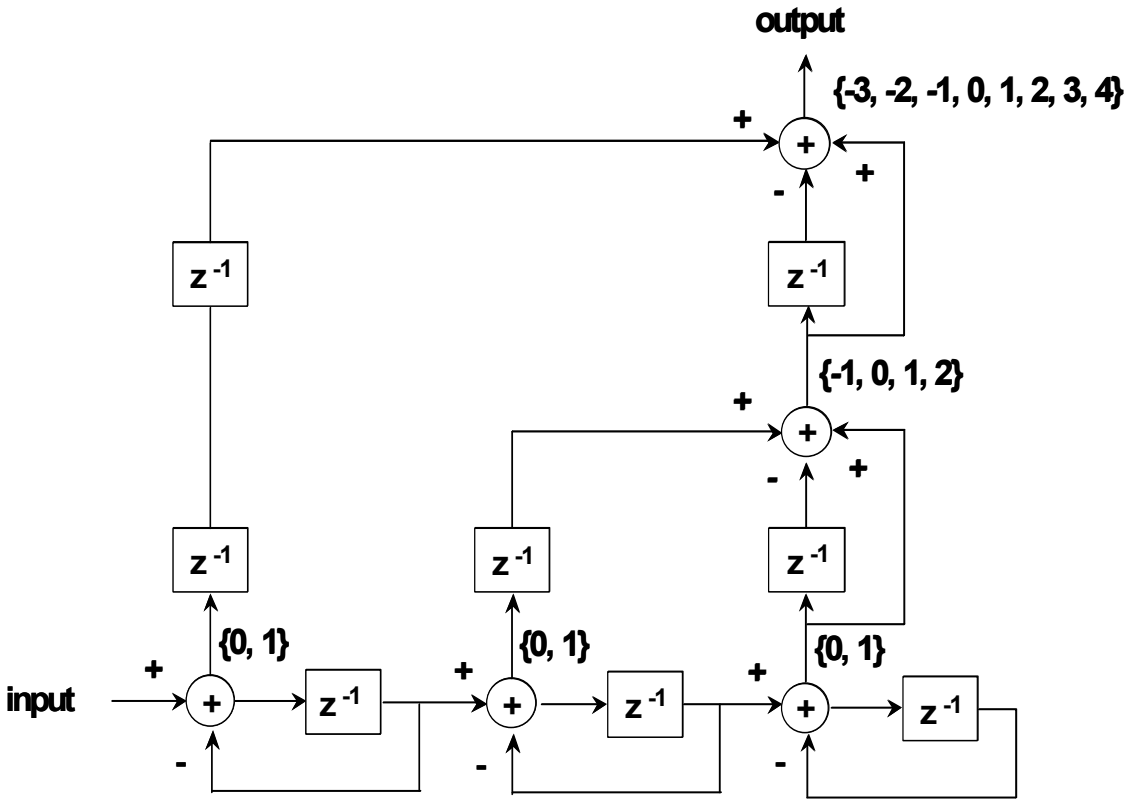


Figure 54. The third-order MASH

In the above equations, G_i indicates the generate signal at the i-th stage and P_i is the propagate signal at the i-th stage of the adder. The sum output is generated by

$$S_i = C_{i-1} \oplus P_i \qquad \text{(eq. 71)}$$

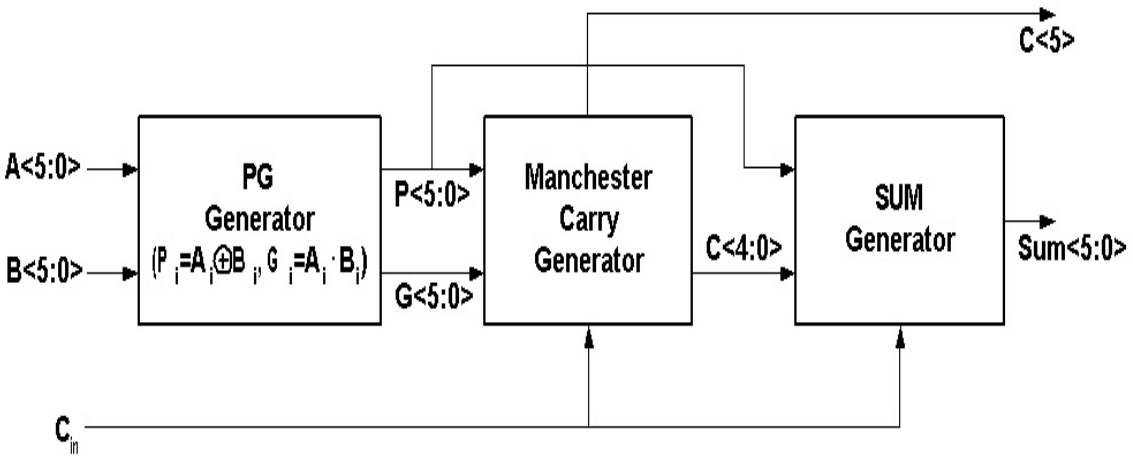


Figure 55. The block diagram of a six-bit Manchester adder

Figure 55 shows the block diagram of the six-bit Manchester adder. From the PG generator, the propagate (P) and the generate (G) signals are produced.

Figure 56 shows the plot of the phase noise vs. the offset frequency based on the center frequency.

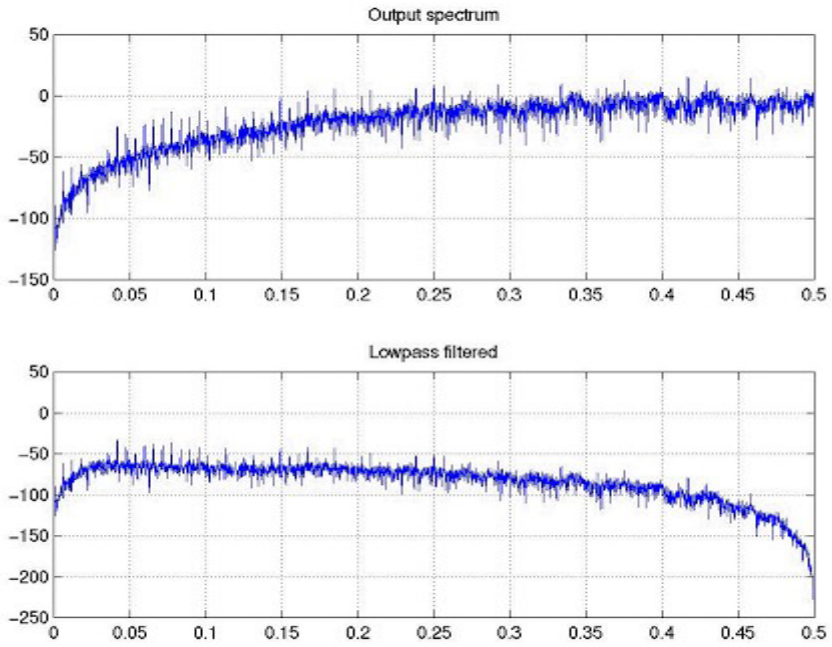


Figure 56. System-level simulation results of the third-order MASH phase noise

4.3.3 Digital-to-Analog Converter

The signal through a digital FIR filter has to be converted to an analog signal to control the Voltage-Controlled Resistor (VCR). Therefore, a Digital-to-Analog Converter (DAC) is required to for the conversion.

In general, the frequency resolution is determined by the resolution of the DAC. However, in the designed frequency synthesizer, the MSB three bits directly control the current of the VCO and only the LSB bits control the VCR. Thus, the eight-bit resolution is enough to meet the Bluetooth application or other general wireless communication specification. The most important static specifications of a general DAC are Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) [23,36]. These nonlinearities are continuously corrected by the feedback loop in the designed frequency synthesizer loop. Therefore, the non-linearity specifications are not important in this application. Instead, the monotonic conversion characteristic is the most important characteristic in the frequency synthesizer application.

Many high-speed DACs have been implemented using a single-stage current cell matrix because the single-stage matrix DAC has fast settling time. However, this architecture requires a complex decoding logic circuit, higher power consumption, and larger chip area. In addition, high-speed operation is not required in this application. So, the DAC used in the designed frequency synthesizer is implemented using an eight-bit DAC with a symmetric two-stage current-cell matrix architecture that consists of a four-MSB current-cell matrix and a four-LSB current-cell matrix. Using this symmetric architecture, the complexity of decoding logic circuits and the number of current sources are reduced [24].

The circuit diagram of the designed eight-bit DAC is shown in Figure 57. In this diagram, the input digital bits (B_0 ~ B_7) are decoded through the row and column decoders to generate the thermometer-code that ensures monotonic operation. Then, the decoded data (R_{2i}, R_{2i+1}, C_j) are passed through the matrix-switching decoders to generate the $V_{o,i,j}$.

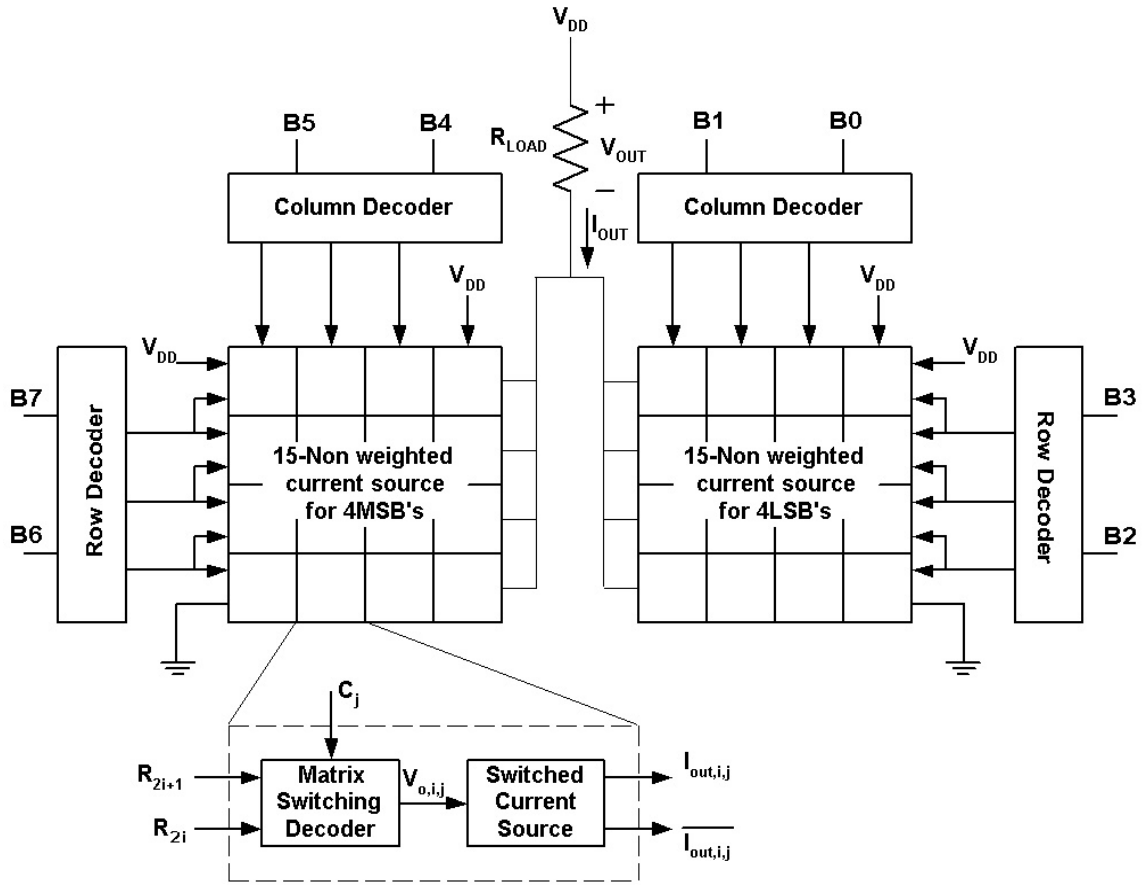


Figure 57. An eight-bit Digital-to-Analog Converter

The $V_{o,i,j}$ signal produced by the matrix-switching decoder is applied to the switched current source, which generates the two current components, $I_{out,i,j}$ and $\overline{I_{out,i,j}}$. The sum of these currents decides the total output current. As a result, the output current I_{out} and the output voltage V_{out} are obtained by equation (72) and equation (73), respectively.

$$I_{out} = I_{MSB} (2^3B_7+2^2B_6+2^1B_5+2^0B_4) + I_{LSB} (2^3B_3+2^2B_2+2^1B_1+2^0B_0) \quad \text{(eq. 72)}$$

$$I_{MSB} = 16\, I_{LSB} \quad \text{(eq. 73)}$$

where B_i = the i-th input digital bit, I_{MSB} = the MSB current, and I_{LSB} = the LSB current

Therefore, the output voltage is given by

$$V_{out} = I_{out} \cdot R_{LOAD} \quad \text{(eq. 74)}$$

where R_{LOAD} is the load resistance.

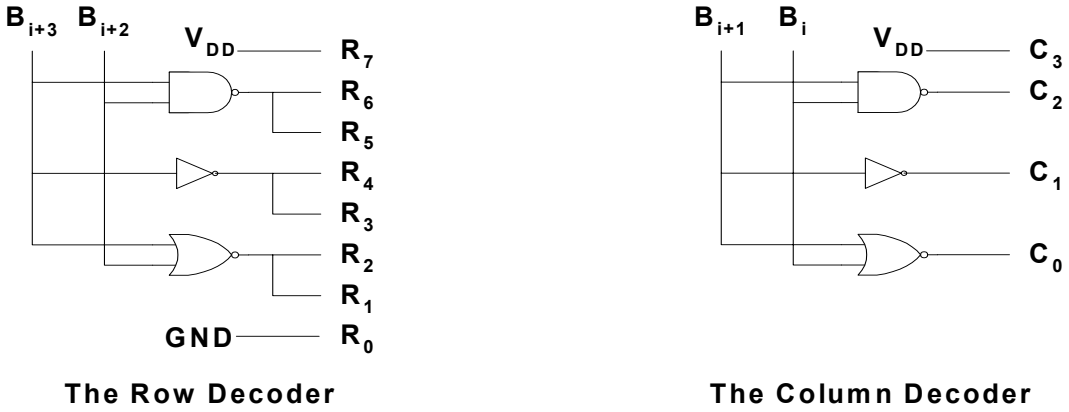


Figure 58. The row and column decoders

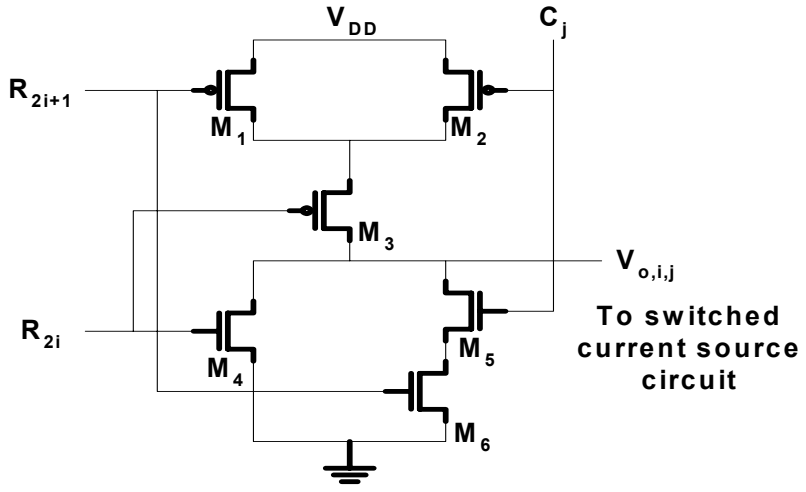


Figure 59. The matrix switching decoder

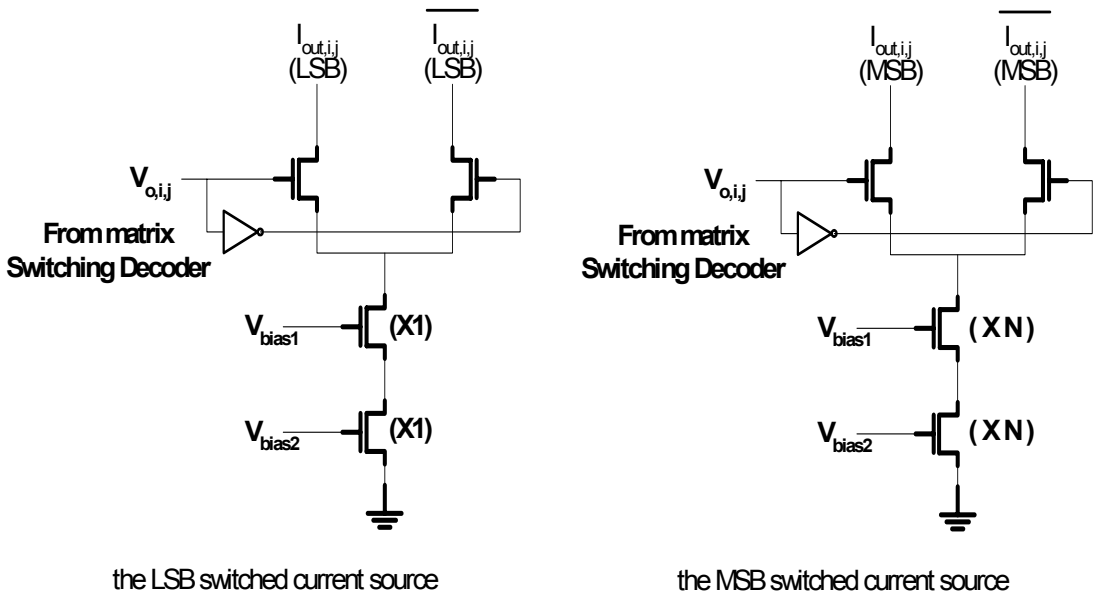


Figure 60. The LSB- and MSB-switched current sources

In Figure 58, the decoders that only use two NAND, two inverter, and two NOR gates are shown. The circuit diagrams of the matrix switching decoder and switched current sources are shown in Figure 59 and Figure 60. From Figure 59, The output voltage $V_{o,i,j}$ of the matrix switching decoder is expressed by

$$V_{o,i,j} = R_{2i} \cdot (R_{2i+1} + \overline{C_j}) = R_{2i+1} + R_{2i} \cdot \overline{C_j} \qquad \text{(eq. 75)}$$

In this equation, the logic state of $V_{o,i,j}$ depends on C_j only if R_{2i} is low and R_{2i+1} is high. This matrix-switching decoder output signal is fed into the switched current source. There are two kinds of current sources; one for LSB-switched current source and the other for MSB-switched current source. The transistor size of the MSB current source is 16 times that of the LSB current source to generate 16 times larger current flow.

In order to check the monotonic characteristic, transient simulation is carried out and the result is shown in Figure 61.

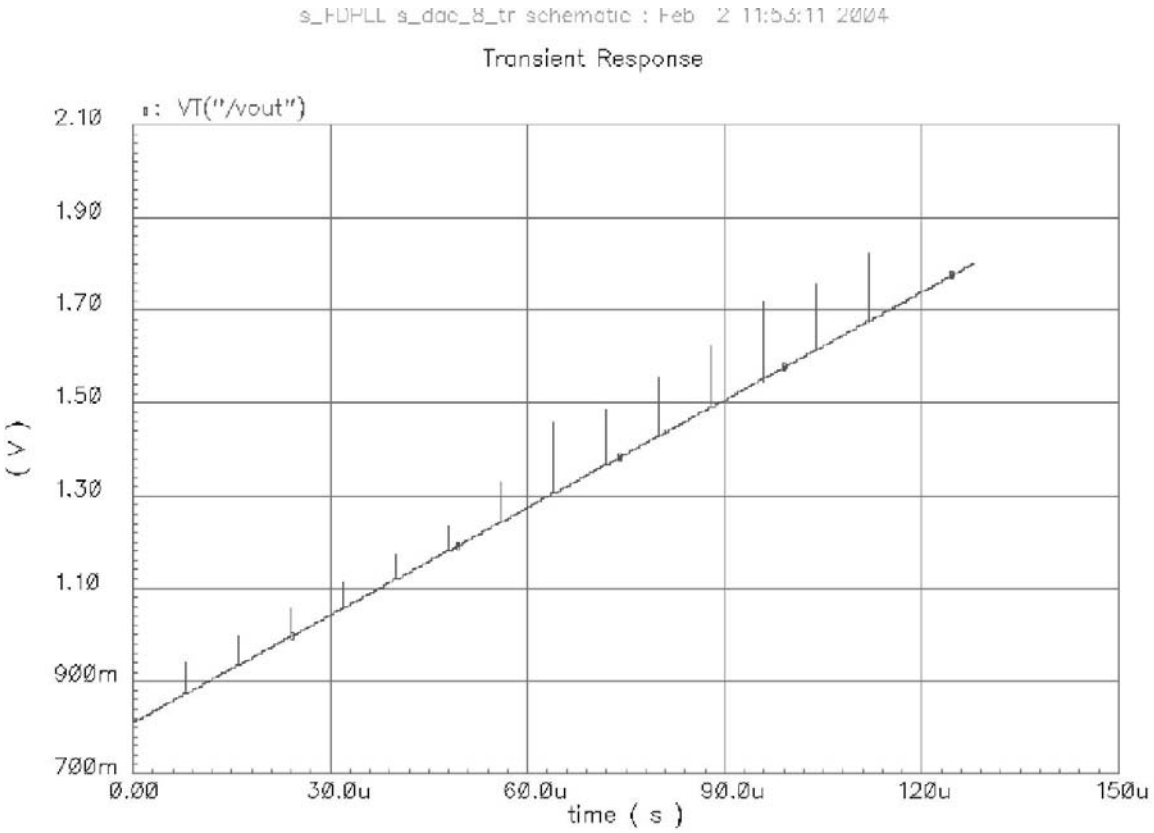


Figure 61. An output waveform of an eight-bit DAC

4.3.4 Prescaler

As discussed in an earlier chapter, a prescaler is needed because developing a FFD that operates reliably at 2.4 GHz or higher is rather difficult. In this design, the prescaler implemented using fixed-rate divider operates at a very high speed. Therefore, the major design requirements are high operating frequency, low power dissipation, and low phase-noise contribution. To meet all the requirements, the prescaler is implemented using a feedback CML that is shown Figure 62.

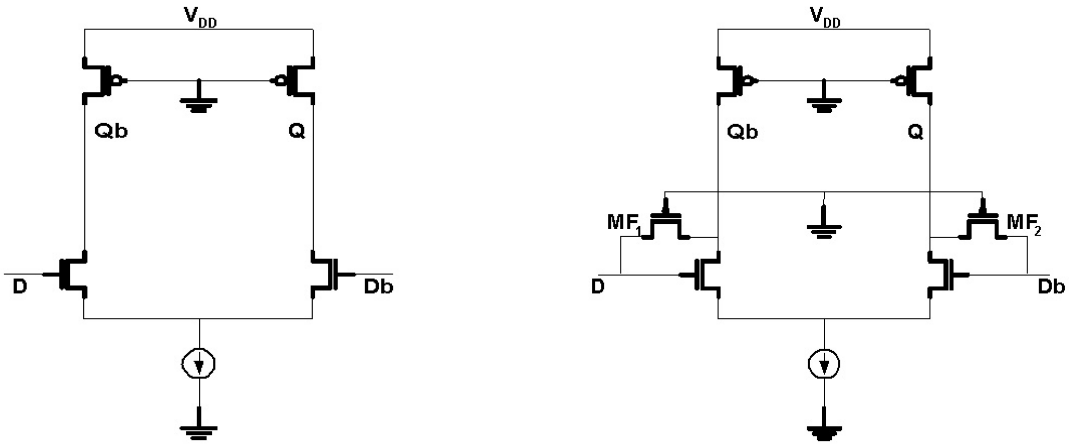


Figure 62. Inverter circuits using CML

(a) Conventional CML (b) Feedback CML

Figure 62 shows the inverters of the conventional and the feedback CMLs. In the feedback CML, transistors MF_1 and MF_2 are added as feedback resistances [25]. Because the conventional CML circuit is a source-coupled pair circuit, the differential-mode voltage gain, $A_d(f)$ is given by [26]

$$A_d(f) = \frac{A_d(0)}{1 - j\cdot\left(\frac{\omega}{\omega_p}\right)} \qquad \text{(eq. 76)}$$

where $A_d(0)$ = the dc gain of the circuit, ω_p = a pole of the circuit, function of the load resistance, and load capacitance of input transistors

If an assumption is made that the feedback transistors have pure resistance only, the gain of the feedback CML is given by

$$A_{feedback}(f) = \frac{A_d(f)}{1 + F_b \cdot A_d(f)} = \frac{A_d(0)}{1 + F_b \cdot A_d(0)} \frac{1}{1 - j\cdot\left(\frac{\omega}{\omega_p}\right)\left(\frac{1}{1 + F_b \cdot A_d(0)}\right)} \qquad \text{(eq. 77)}$$

where F_b = the gain of the feedback transistors

If the loop gain $F_b \cdot A_d(0)$ in equation (77) is zero, then equation (76) and equation (77) become the same. However, if $F_b \cdot A_d(0)$ is greater than zero, then equation (77) becomes the feedback CML gain. In this equation, the bandwidth of the feedback CML is wider than the bandwidth of the conventional ECL-liked Current Mode Logic (CML) because the location of dominant pole is changed to $\omega_p \cdot (1 + F_b \cdot A_d(0))$ from ω_p where $F_b \cdot A_d(0)$ is larger than zero.

In addition to wider bandwidth, the feedback CML has another advantage related to noise problem. When a deep sub-micron transistor is used, the threshold voltage, V_{th} fluctuation caused by the fluctuation of the gate oxide and the random channel dopant is a significant problem in circuit design. If the fluctuation of the threshold voltage is much smaller than the gate voltage, then the bias offset voltage of the circuit is given by

$$\Delta V_{bias\_offset} = - \frac{dI_D}{dV_{th}} \Delta V_{th} R_L = g_m R_L \Delta V_{th} = A(0) \Delta V_{th} \qquad \text{(eq. 78)}$$

where V_{th} = threshold voltage of load transistor, R_L = load resistance, and g_m = transconductance of transistor

From equation (78), ΔV_{bias_offset} is proportional to the dc gain, A(0). Therefore, a small dc gain is better than a large one. If the maximum bandwidth is the same, then the dc gain of the feedback CML is smaller than that of the conventional CML. Thus, the effect of the fluctuation is reduced when the feedback CML is used.

The D flipflop used in the prescaler is shown in Figure 63. This D flipflop uses the feedback CML to get a wide bandwidth and a reduced V_{th} fluctuation effect.

The transient simulation is carried out to check performance of the designed prescaler. The output waveform is shown in Figure 64.

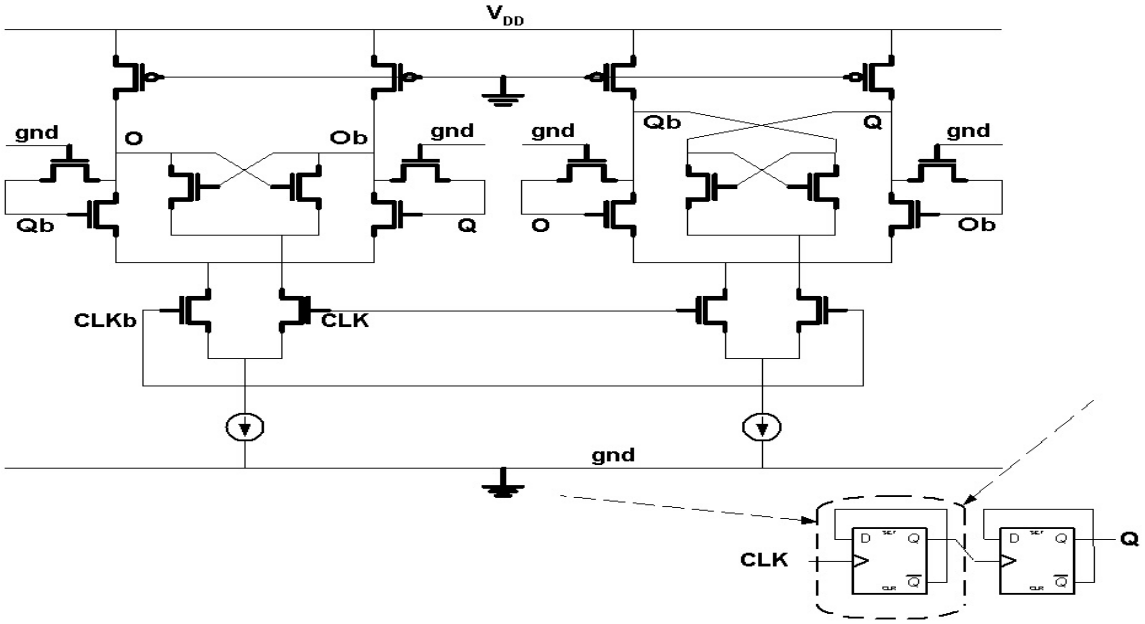


Figure 63. A D flipflop that is used in the prescaler

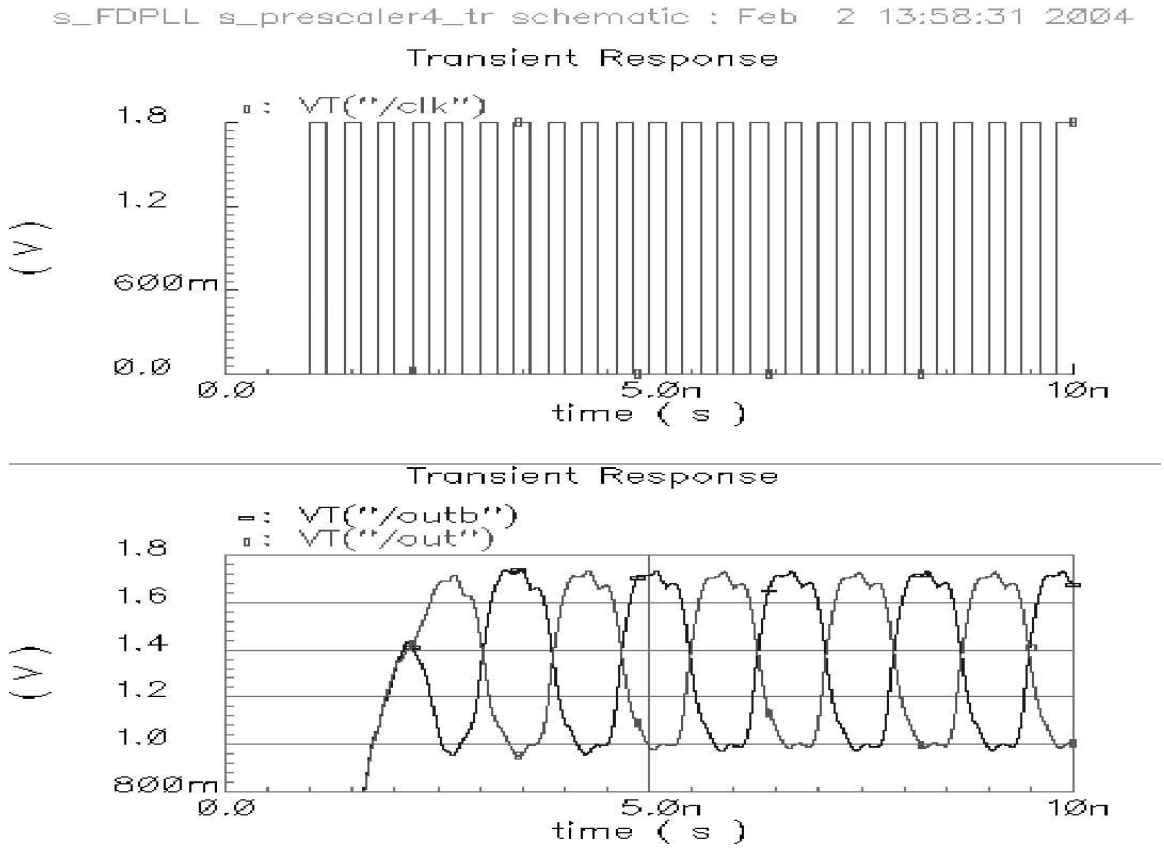


Figure 64. The transient simulation result of the designed prescaler

4.3.5 Voltage Controlled Oscillator (VCO)

LC-tank oscillators have shown good phase-noise performance with low power consumption. However, there are some disadvantages such as narrow tuning range, high phase noise performance dependency on the quality factor of on-chip spiral inductors that is not easily obtained in conventional CMOS technology. So, the VCO used in this design is a two-stage ring oscillator that consists of a couple of delay cells. This type of VCO is preferred because of its low power-dissipation characteristic, small die size, wide operating frequency range, and minimized phase noise [27,28]. In this VCO, the coarse oscillation frequency is controlled by the three-bit digital input signal from the accumulator and the fine oscillation frequency is controlled by the analog input signal from the DAC as shown in Figure 45. These signals control the amount of the source current that decides the oscillation frequency through the VCR control. The VCO also has a reset function required for the phase acquisition. The designed ring oscillator and its delay cell circuit diagrams are shown in Figure 65 and Figure 66.

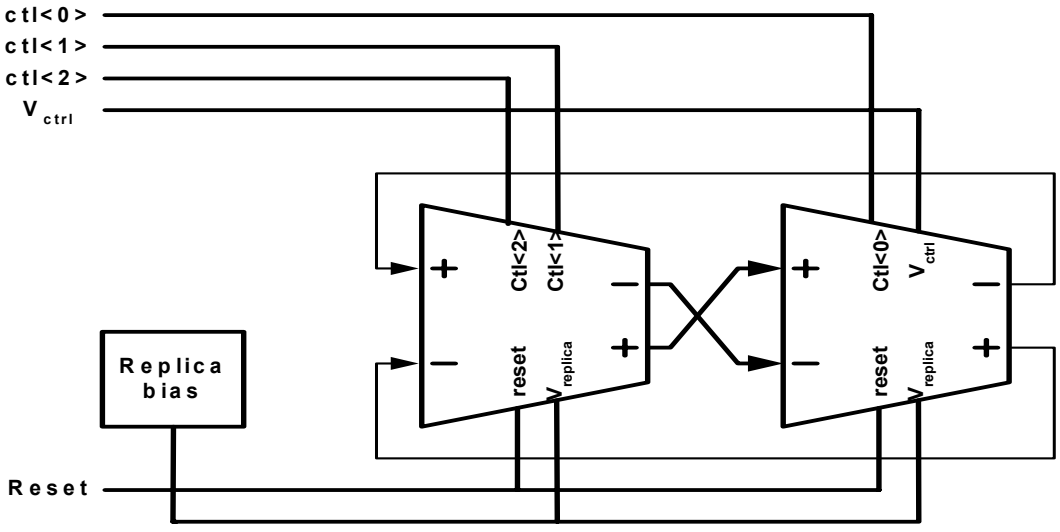


Figure 65. A voltage-controlled oscillator

As shown in Figure 66, the delay cell consists of one NMOS input pair (M_{n1}, M_{n2}), one diode-connected PMOS pair (M_{d1}, M_{d2}), one PMOS pair for frequency tuning (M_{b1}, M_{b2}), one PMOS positive feedback pair (M_{p1}, M_{p2}), and one NMOS pair for reset (M_{r1}, M_{r2}).

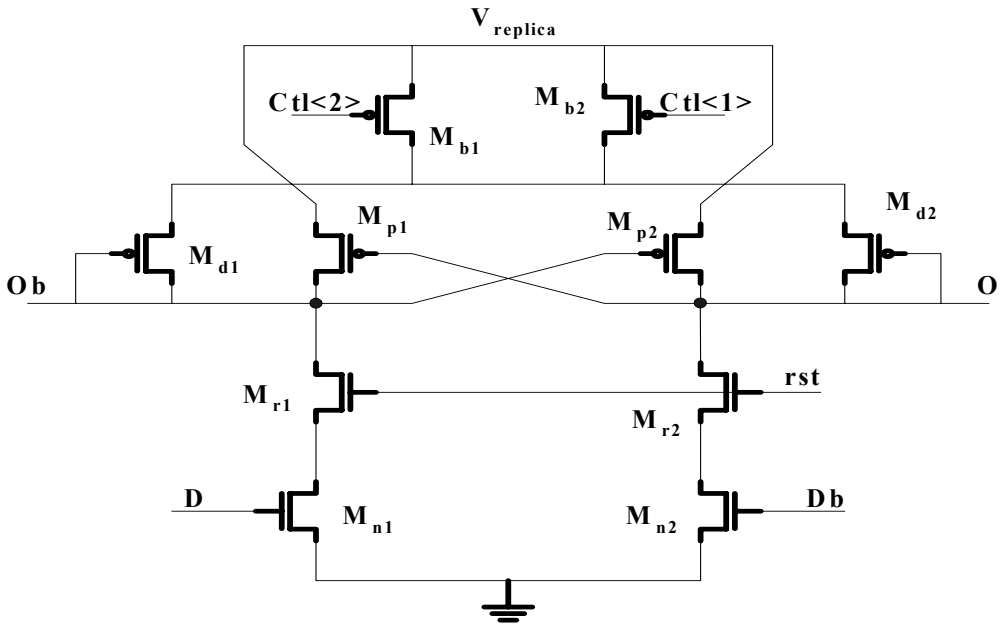


Figure 66. A delay cell used in the VCO

In this delay cell, instead of a PMOS input pair, an NMOS input pair is used to maximize the transconductance-to-capacitance ratio so as to achieve high operating frequency with low power dissipation. In order to reduce the g_m requirement and power dissipation, only parasitic capacitors of delay cell are utilized.

To support multi-mode and multi-application, large tuning range is required. In this design, frequency tuning is achieved by tuning the transconductance, g_m, of the diode-connected PMOS devices, M_{d1} and M_{d2}. By controlling the current of M_{b1} and M_{b2},

the g_m of M_{d1} and M_{d2} can be adjusted from zero to g_m of M_{p1}. In this manner, larger tuning range can be achieved.

From the Barkhausen oscillation maintain requirement of ring oscillator, the oscillation frequency of the designed ring oscillator can be derived

$$f_{osc} = \frac{1}{2\pi} \cdot \sqrt{\frac{g_{mn1}{}^2 - (-g_{mp1} + g_{md1} + G_L)^2}{C_L{}^2}} \qquad \text{(eq. 79)}$$

where $G_L = g_{dn1} + g_{dp1} + g_{dd1}$ at g_d is the channel conductance

C_L = parasitic cap of transistors and g_{mr1} is ignored

So, the output frequency f_{osc} can be tuned by controlling the g_m of diode-controlled PMOS devices, as discussed earlier.

The phase-noise and transient simulations of the designed VCO is carried out and shown in Figure 67 and Figure 68. In Figure 68, the reset function test is also carried out.

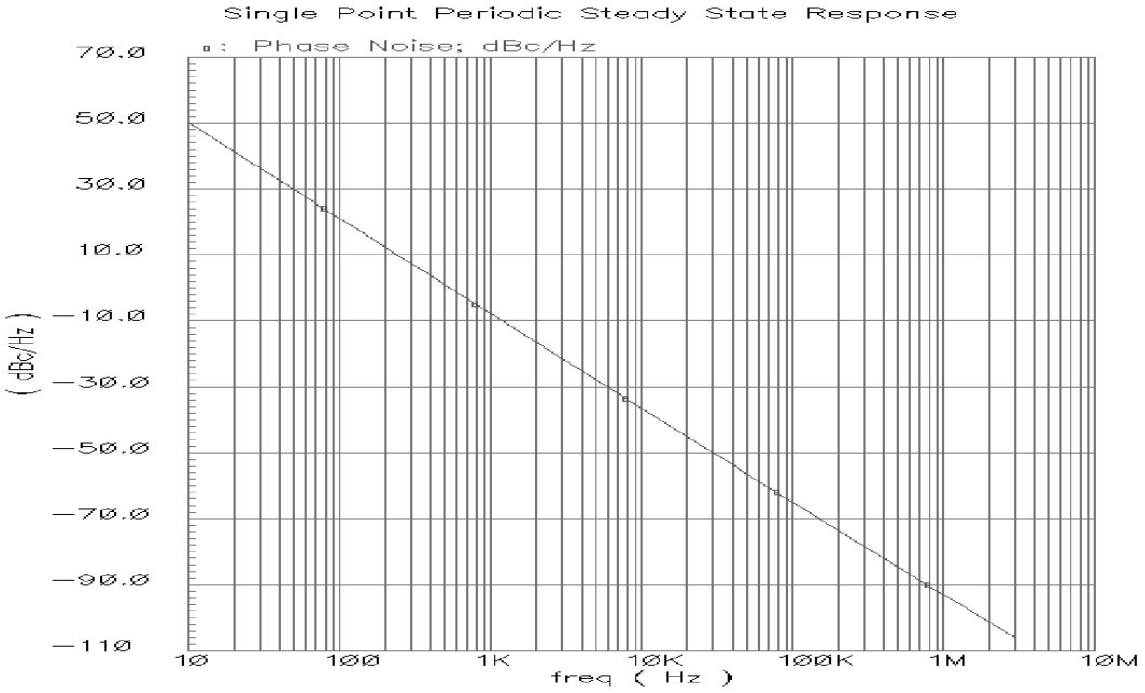


Figure 67. The phase noise simulation result of the designed VCO

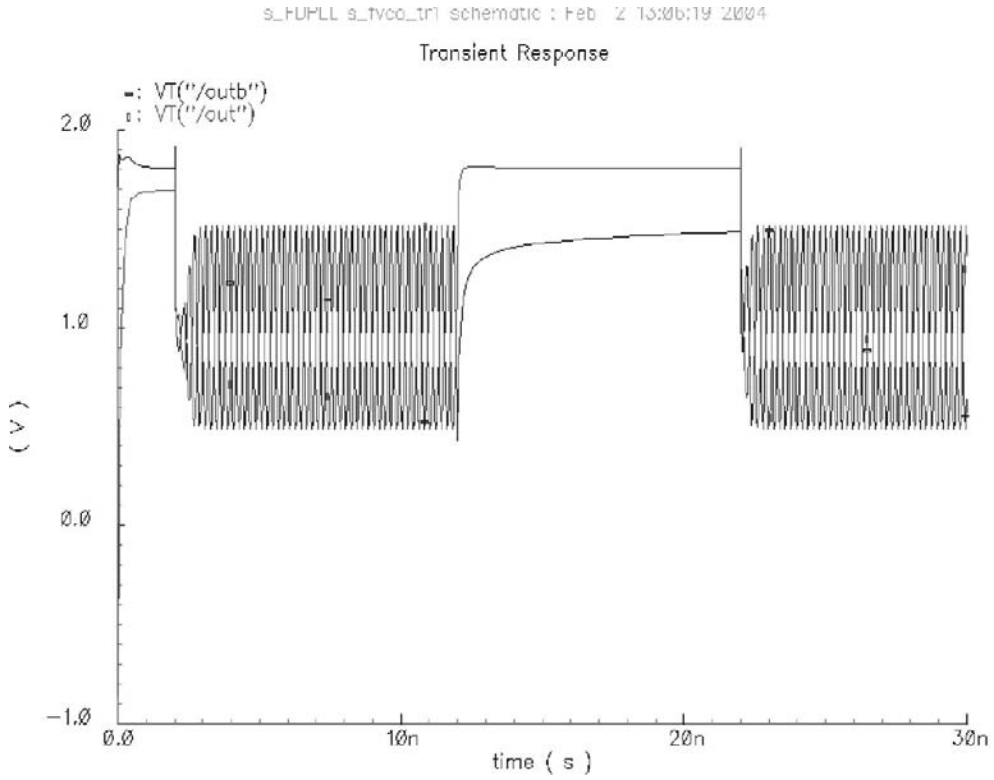


Figure 68. The transient simulation result of the VCO

4.3.6 Digital FIR Filter

In general, the loop filter in the frequency synthesizer is implemented using passive elements. However, the performance of the analog loop filter is sensitive to process and temperature variations and aging. Therefore, in this design, an analog loop filter is replaced with a programmable digital Finite Impulse Response (FIR) filter. Figure 69 shows a signal-flow graph of the nth-order FIR filter, but the structure shown in Figure 69 requires too many multipliers that result in a large area and a high power dissipation.

To reduce the complexity of a FIR digital filter, its coefficient is encoded using the Canonic Signed-Digit (CSD) code, i.e., numbers that can be represented as sums or differences of powers of two. Using the CSD coding technique, the multipliers are

replaced by simple barrel shifters. Additionally, using either symmetric or anti-symmetric coefficients, the multipliers can be shared, as shown in Figure 70 [29.30]. Therefore, the number of multipliers and the coefficient routing are reduced by about one-half. In this design, the CSD coding technique is used. Thus, the number of barrel shifters is reduced in the same way the multipliers were reduced in Figure 70.

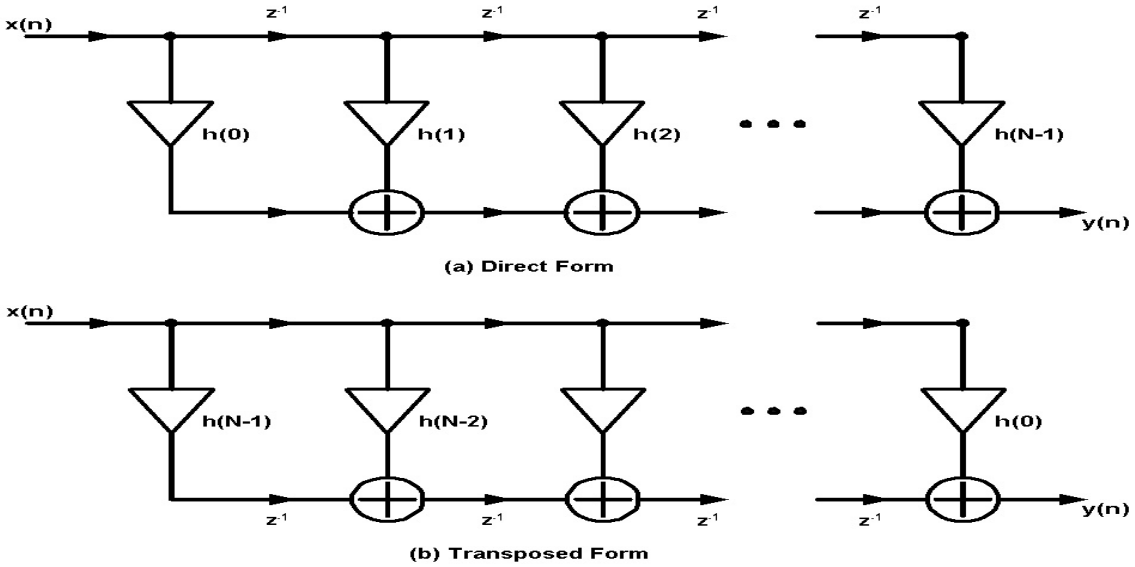


Figure 69. Signal flow graph of nth-order FIR filter

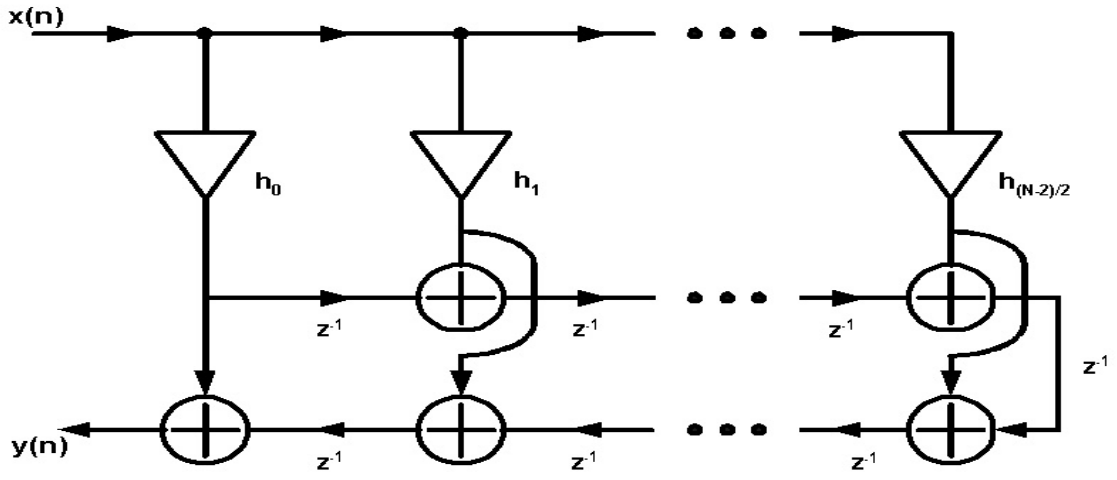


Figure 70. Linear phase transpose direct form filter structure

The coefficients of the required digital filter are obtained using Matlab® simulation and those coefficients are shown in Table 3.

Table 3. Coefficients of the designed FIR filter

Coefficient	Value	Coefficient	Value
h(0)	.0047600686	h(5)	.2155474163
h(1)	.0344538548	h(6)	.1123841387
h(2)	.1123841387	h(7)	.0344538548
h(3)	.2155474163	h(8)	.0047600686
h(4)	.2657149057		

The frequency response of the designed filter is shown in Figure 71. Using the coefficients of Table 3, the FIR digital filter is synthesized using Synopsys® synthesis tool. The circuit diagram that is synthesized with the logic library of the National semiconductor is shown in Figure 72.

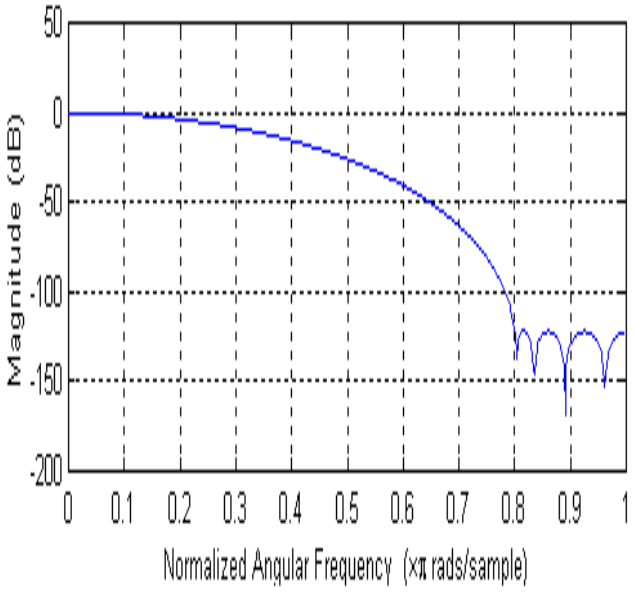


Figure 71. The frequency response of the designed filter

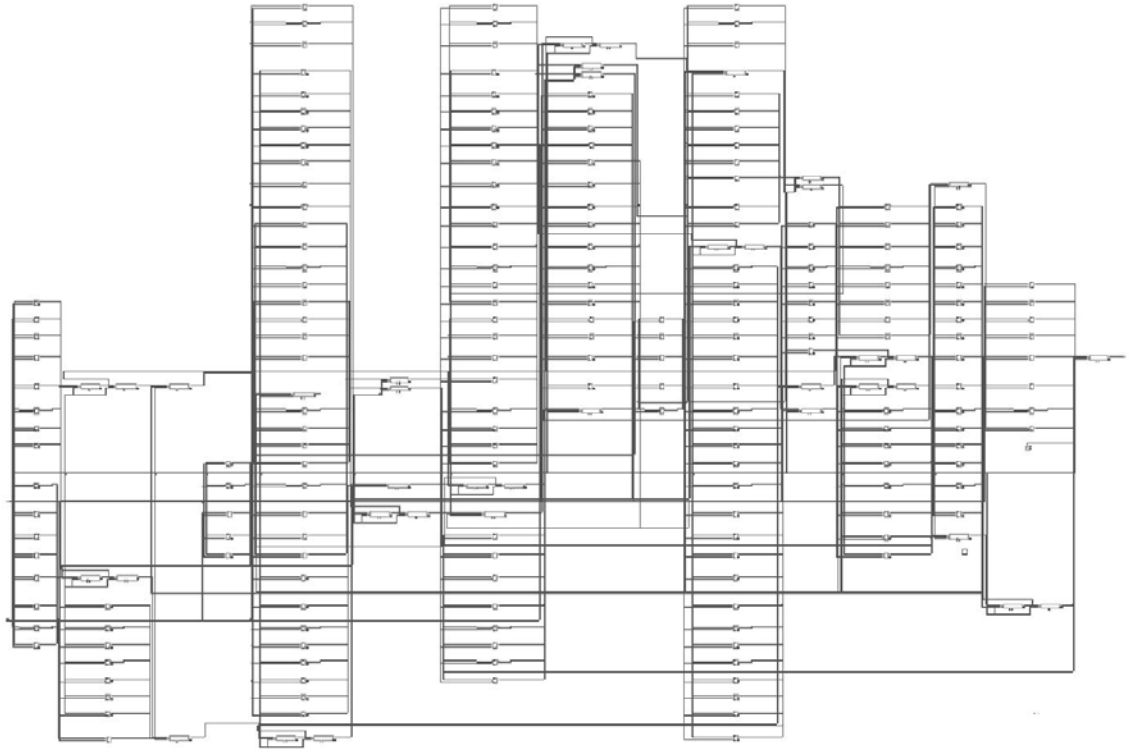


Figure 72. The synthesized FIR digital filter

4.4 Conclusion

In this chapter, the design details of a fully integrated, fast-locking fractional-N frequency synthesizer has been discussed at both the system and circuit levels. In this frequency synthesizer implementation, passive elements such as large and inaccurate capacitors and resistors in a loop filter have been substituted by a programmable digital Finite Impulse-Response (FIR) filter. Second, the adaptive loop-gain control proportional to the frequency difference was used to make frequency locking time fast. Lastly, the phase noise and spurs have been reduced by a MASH controlled FFD that generates a digital output corresponding directly to the frequency difference. So, the

frequency synthesizer designed for this thesis offers a high integration ability, technological robustness, fast locking time, low noise level, and multi-mode flexibility.

To prove performance of the newly designed frequency synthesizer, system-level simulations have been carried out using Matlab® by applying the Bluetooth application standard. The circuit-level simulations of each block needed to implement have been also performed using SpectraRF®.

Chapter 5

Measurement of Frequency Synthesizer

In this chapter, the experimental preparation such as the selection of electronic components, the schematic of test circuit, Printed Circuit Board (PCB) layout, and testing equipment set-up for three test circuits that are prepared to measure the three designs including a fully integrated frequency synthesize, a VCO, and a frequency synthesizer (excluding digital FIR loop filter) are covered. Then, the experimental results including phase noise of a fully integrated frequency synthesizer are summarized.

5.1 Measurement Set-up

Three prototypes have been fabricated using a 0.18 um CMOS technology with five metal layers. A fully integrated frequency synthesizer has been implemented in the first version. The second version includes a VCO that has been used in the first version. In the third version, a frequency synthesizer that does not include a FIR loop filter has been implemented. So, as shown in Figure 73, three kinds of test circuits have been prepared to test each prototype.

Each test circuit has the power-supply decoupling network that consists of an 18 Ω series resistor and four surface-mounted, low capacitance-variation, low temperature-variation, low-inductance ceramic capacitors. These power-supply decoupling components should be placed as close to the tested device power pins as possible to reduce noise coupling.

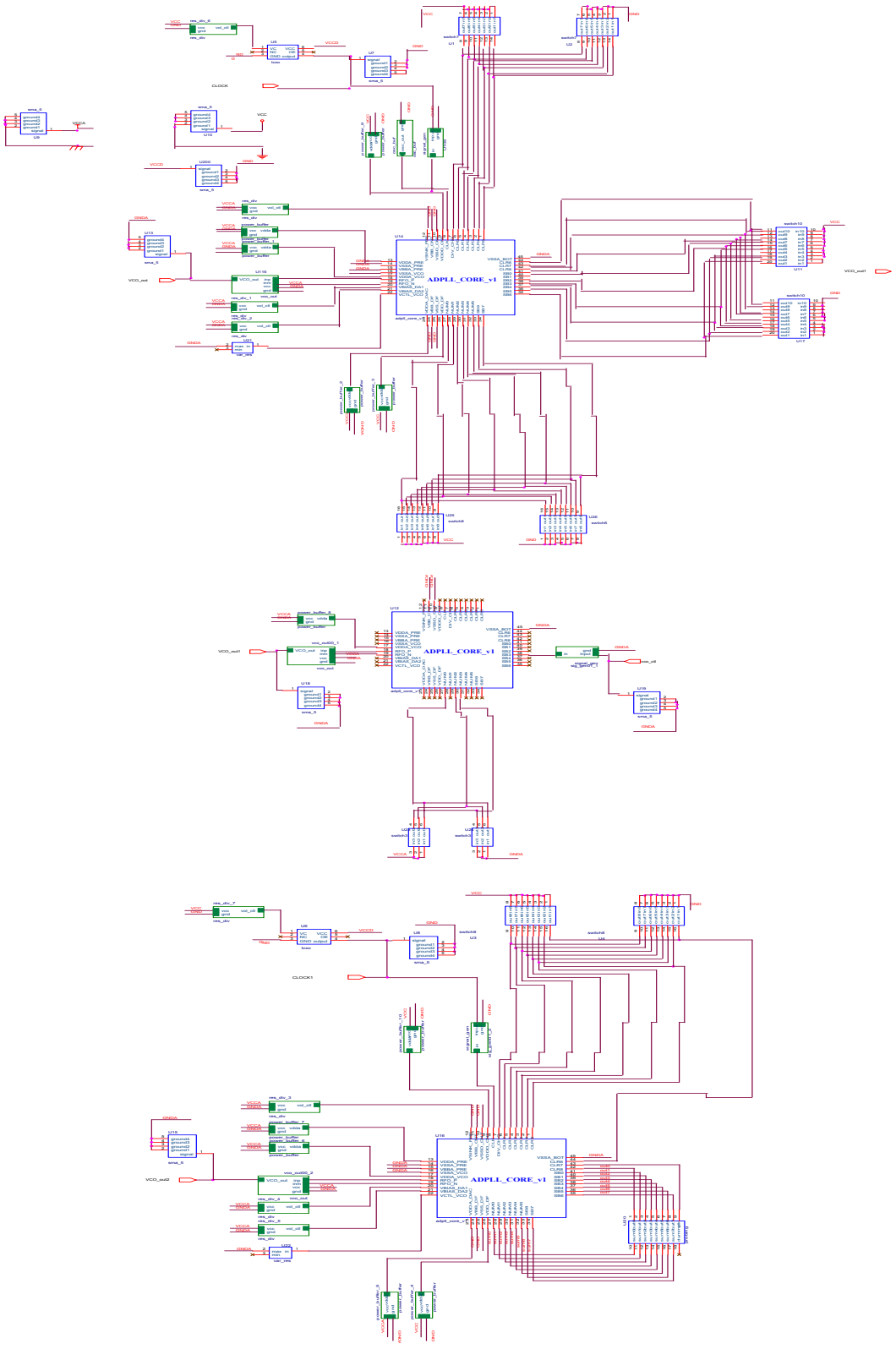


Figure 73. Schematic of test circuits

Analog power pins and digital power pins have the same power- supply decoupling networks.

For the purpose of reducing the noise-coupling, low-inductance ceramic capacitors are used for each pin, which feeds DC control signals into the designed chip or sets up bias voltage or current for the designed circuit.

Switches are placed on the testing circuit to set the digital control signal of the MASH that controls the division ratio of divider and the initial value of FFD. SMA connectors are used to monitor or feed the signals at the appropriate pins and power.

One of the three input source options including a signal generator pulse output, a crystal oscillator output, and a low frequency, low phase-noise discrete VCO output can be used as a reference frequency signal to obtain best performance.

A head connector has been used to manipulate the output signal of the third prototype version without an internal, digital FIR loop filter. Using this connector, the loop filter function can be carried out by PC software or FPGA.

5.2 PCB Design

In general, a four-layer PCB board has been used for high-speed, high-resolution applications and radio frequency, low-noise applications to minimize noise due to power supply noise and pick-up noise from other parts. In addition, the four-layer board allows a whole layer to be devoted as a ground plane or power plane without any disruption by signal crossovers. Therefore, a four-layer PCB board is used to implement test circuits for this thesis. The test circuit schematic design and PCB layout have been completed using OrCad Layout Plus®.

Among four layers, the second layer and the third layer from the top layer are usually used as a ground plane and a power plane, respectively. The other two layers are used for signal routing as shown in Figure 74. Once the planes are arranged, the PCB layout follows these rules. First, partition each plane by its circuit function such as power, ground, DC signal manipulation, AC signal manipulation, RF function, etc. Second, isolate critical analog signal or RF signal paths from digital signal. Third, isolate high frequency circuits from low frequency or DC ones. Fourth, place noise-coupling components as close to the DUT as possible. Fifth, make the high frequency or analog signal routing as short as possible. Sixth, route critical paths by hand rather than by automatic signal-routing CAD layout software.

Impedance matching is the one of the most important issues when the frequency synthesizer is designed and tested. If the frequency synthesizer impedance differs from the trace impedance, then power will be reflected back towards the frequency synthesizer, and a significant power will be lost.

The characteristic impedance of the trace between the DUT and other components on PCB is determined by the width of the trace, W, the height of the trace above the ground plane, H, and the relative dielectric constant, ε_r, of the material used for the PCB board. Because the trace impedance is almost independent of frequency, the trace impedance can be calculated with the following formula:

$$Z_o = \sqrt{\frac{L}{C}} = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \bullet \ln\left(7.5 \bullet \frac{H}{W} \right) \qquad \text{(eq. 80)}$$

where L = the inductance per unit length

C = the capacitance per unit length

From the equation (80), the ratio of the height to the width is about 0.5 for 50 Ω trace. In other words, if the thickness from the top layer to the ground plane is 30 mils, then the width of the trace should be 60 mils for impedance matching in FR-4 type four-layer PCB.

All components that are used in test circuits are selected from the surface-mounted components in order to reduce parasitic components such as capacitance, inductance, and resistance.

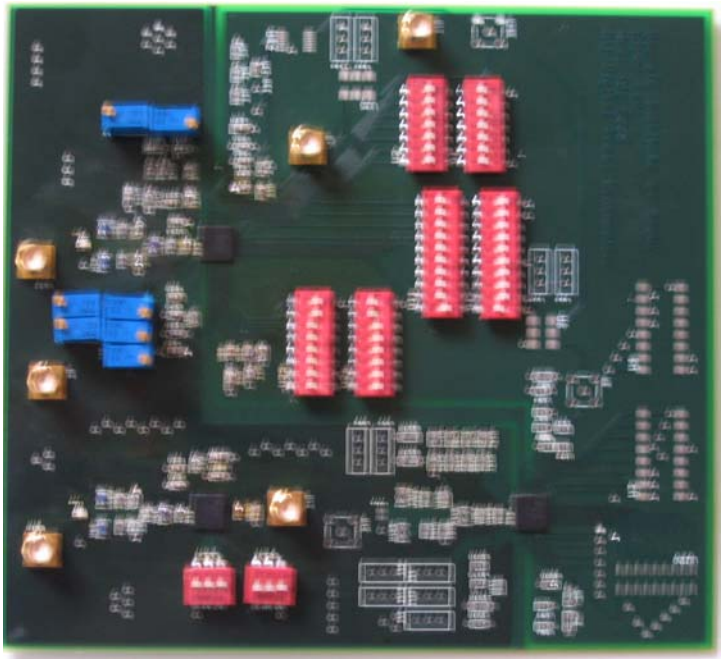
The RF output has 50 Ω source termination for driving a 50 Ω cable through the output SMA connector.

As discussed earlier, the top and bottom photographs of the PCB is shown in Figure 74.

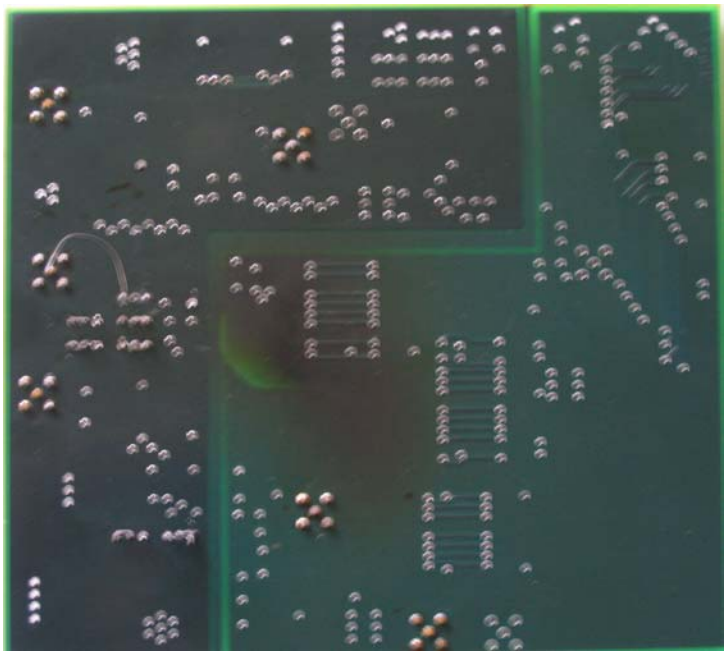
5.3 Test Instruments

The following equipments have been used to test the three versions of designed circuits. Specifically, the spectrum analyzer has been used to measure the phase noise performance.

- Four layer, FR-4 type PCB
- Rhode & Schwarz spectrum analyzer FSU (20 Hz ~ 8 GHz)
- HP E3631A & HP 6237B triple output DC power supply
- HP 8165A programmable signal source
- HP 54602B oscilloscope
- Tektronix TDS 7154 digital phosphor oscilloscope
- HP E2373A multi-meter



(a)



(b)

Figure 74. Photographs of the top (a) and bottom (b) sides of PCB

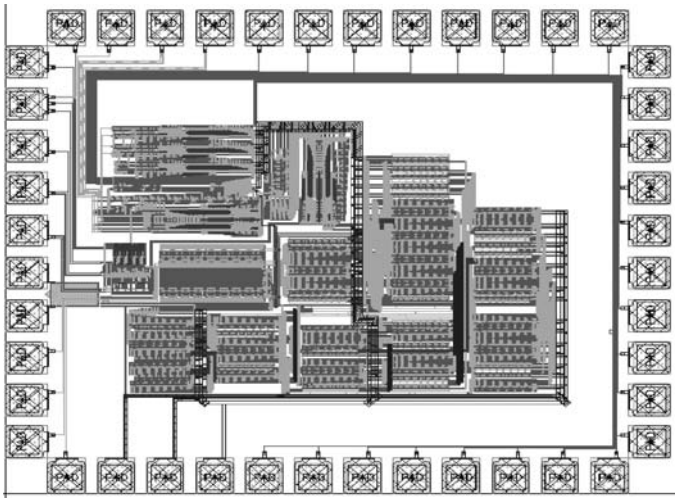
5.4 Experimental Results

As discussed earlier, the three prototypes have been fabricated using a 0.18 um CMOS technology with five metal layers. Each prototype layout has been drawn as shown in Figure 75, using Cadence® Virtuoso layout tool. The pad-included chip area for the first prototype is 1137 um * 1148 um and the area of the second version that includes only a VCO is 446 um * 346um. The pad-included chip area for the third prototype is the same with the area for the first prototype.

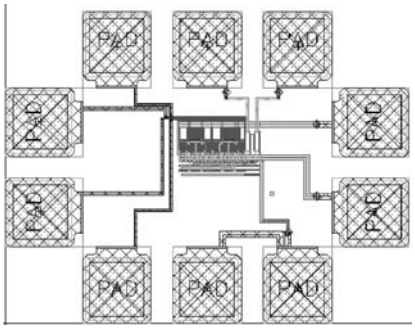
All the chips are packaged in a National semiconductor's 44-pin Leadless Lead-frame Package (LLP), which has very small bond-wire inductance to RF output pins and RF grounds, as well as very small substrate resistance, inductance, and capacitance. In general, this package can be used up to 10 GHz RF territories without serious performance degradation caused by its parasitic.

The total current consumption of the first prototype is 19.2 mA for a 1.8 V power supply voltage. Almost all of the current consumption is used for a VCO, a VCO buffer, and a prescaler. The photograph of the fabricated, fully integrated frequency synthesizer is shown in Figure 76.

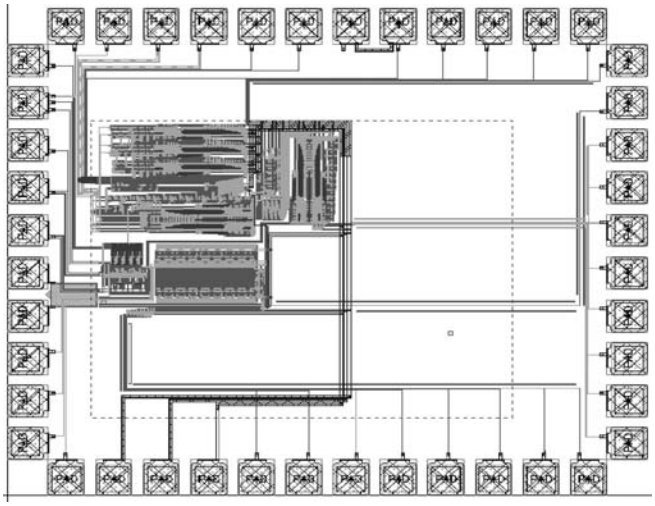
Figure 77 shows Rhode & Schwarz spectrum analyzer measurements of the RF signal output. A reference signal frequency, F_{ref}, with a 2 MHz frequency and –10 dBm signal power was applied to the reference input port using a HP 8165A programmable signal source. This reference signal is divided by two using the reference divider then used as an internal reference signal for FFD, MASH, digital loop filter, DAC, and accumulator.



(a) A fully integrated frequency synthesizer



(b) A VCO



(c) A frequency synthesizer without internal digital filter

Figure 75. Layout diagrams of three test circuits

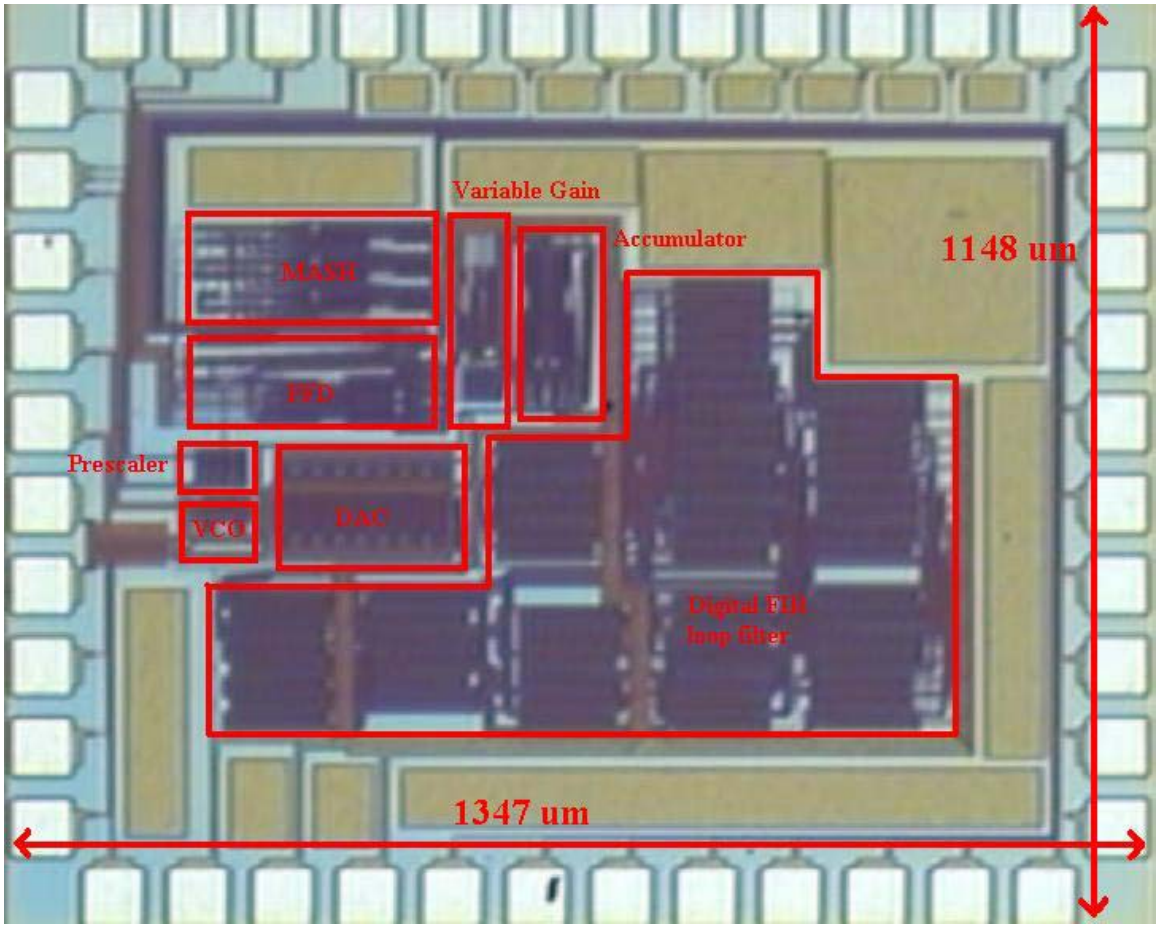
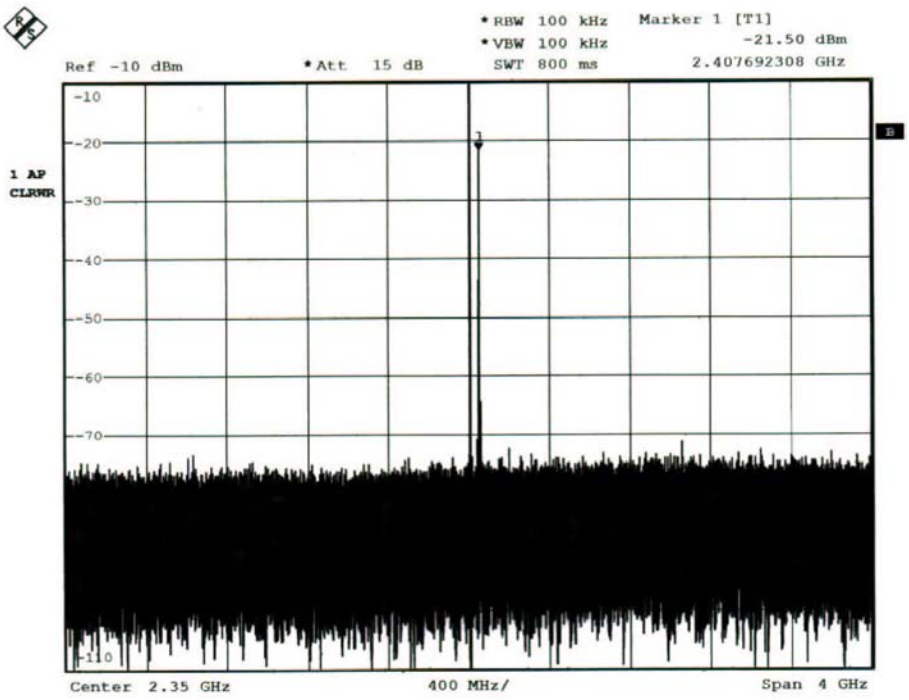
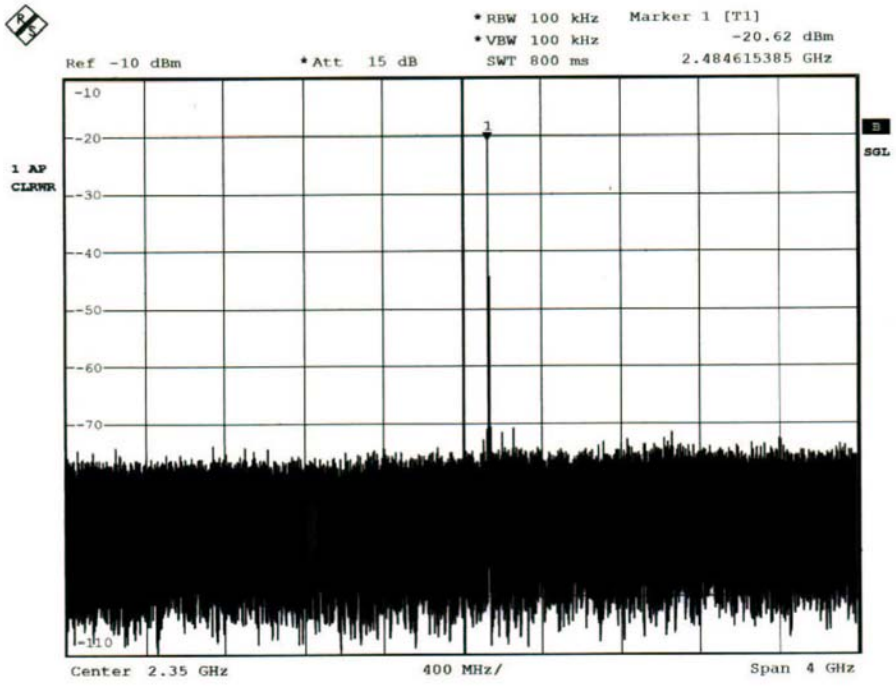


Figure 76. The chip photograph of the fully integrated frequency synthesizer

Figure 77 (a) is the measured spectrum result when the center frequency, f_c is set to 2.4 GHz by forcing data '0001 1100 0010' as an initial value of the FFD and '0' as a numerator value of the MASH. Figure 77 (b) shows the output spectrum when the initial value of FFD is set to '0001 1101 0001' and the MASH fractional data is set to '55' by external switches. The center frequency is equal to f_c = {465 + (55/64)} * {4 * (4/3) * 1 MHz} = 2.4846 GHz. The fabricated frequency synthesizer's tuning range meets the specification of Bluetooth that was targeted in this thesis. However, the actual tuning range of the implemented VCO is almost 50 %. Therefore, the implemented frequency synthesizer can be easily adaptable in multi-mode, multi-application.



(a)



(b)

Figure 77. RF output spectrums at (a) 2.4 GHz and (b) 2.48 GHz

Figure 78 and 79 show the measured phase-noise, which is also measured using the Rhode & Schwarz spectrum analyzer when the center frequency is set to 2.4 GHz. The measured phase-noise is –102 dBc/Hz at a 2 MHz offset and the sideband spurious tone is less than – 48 dBc.

Because the effects of close-in VCO phase noise can be minimized if PLL loop bandwidth and phase comparison frequency can be kept high, a fractional-N frequency synthesis technique can be utilized along with a ring oscillator VCO to produce the required local signal for the system. So, in order to reduce the VCO phase noise and the digital filter area, the wide-bandwidth, low-order loop filter has been used as shown in Section 4.3.6. However, the high frequency noise power occurring in MASH and the in-band noise coming from the reference signal are not suppressed well enough due to the wide-bandwidth, low-order loop filter.

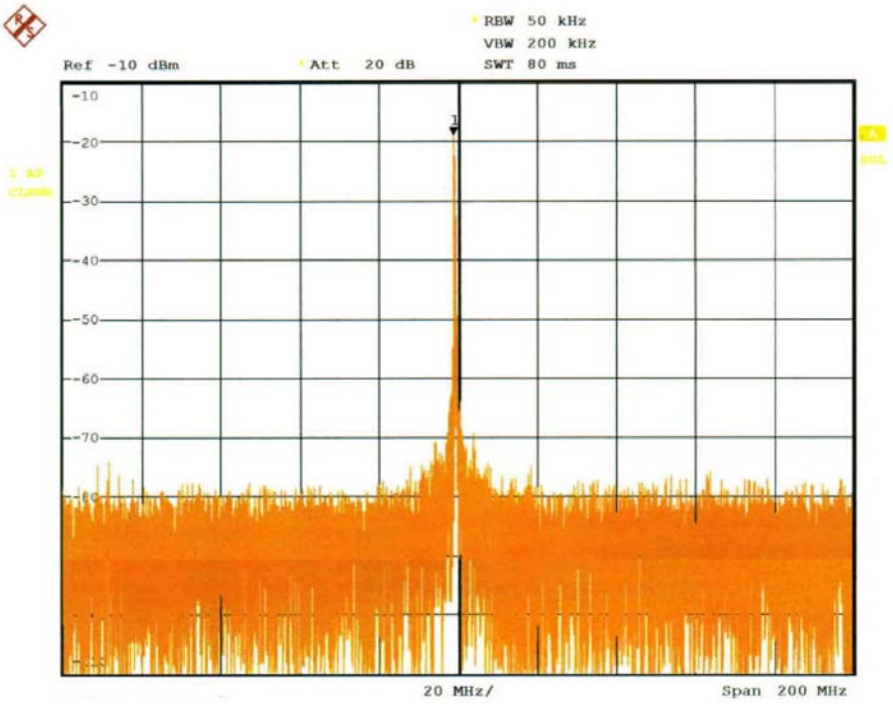


Figure 78. The RF output spectrum with 200 MHz span

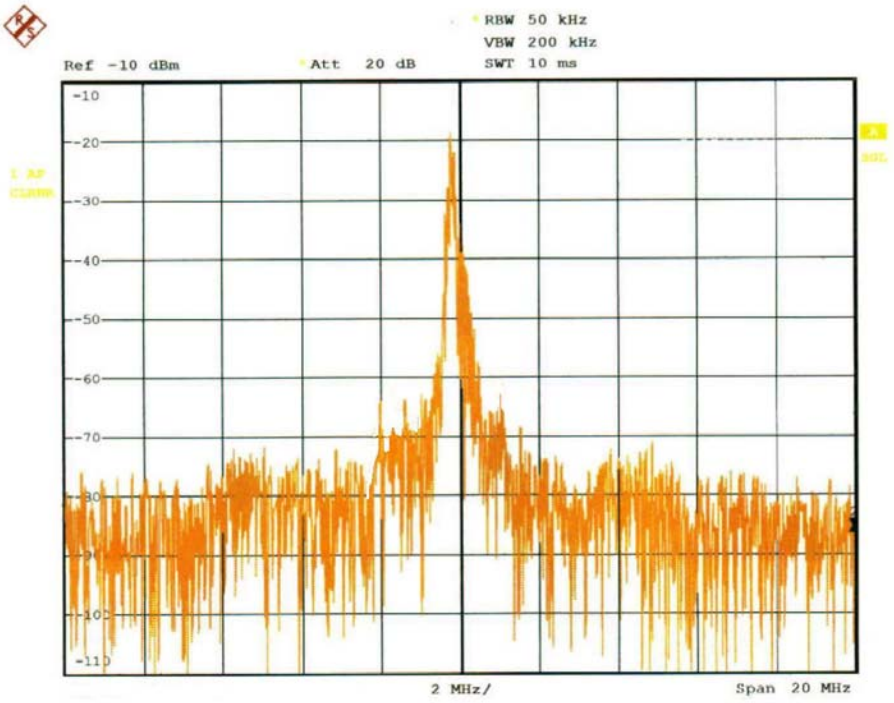


Figure 79. The RF output spectrum with 20 MHz span

Therefore, to reduce the phase-noise degradation caused by high-power noise coming from the noise shaping in the MASH and the reference signal, the loop filter's bandwidth needs to be narrower. Another source of phase noise degradation is substrate noise coming from the digital circuits on the fabricated chip.

Figure 80 shows the harmonic distortion of the RF output. The measured second harmonic is –17 dBc. The second harmonic is degraded by the sampling between digital loop filter and eight-bit DAC and by the impedance mismatching at the RF output due to the larger parasitic elements.

5.5 Conclusion

The three prototypes have been designed and fabricated using a 0.18 um CMOS technology with five metal layers. The version two and three that were fabricated in Jan. 2003 have not worked. Only the fully integrated frequency synthesizer that was fabricated in July 2003 has worked successfully.

The pad-included chip area for the first prototype is 1137 um * 1148 um and the chip consumes 19.2 mA for a 1.8 V supply voltage. The phase noise at a 2 MHz offset is –102 dBc/Hz. The frequency operating ranges are 2.4 GHz ~ 2.4853 GHz. The reference sideband spurs are – 48 dBc.

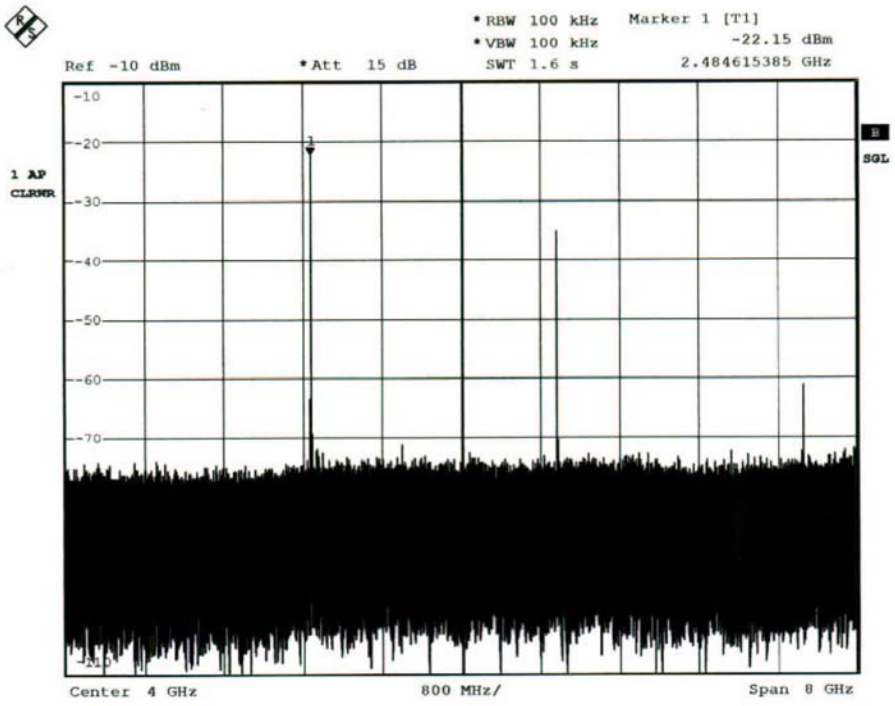


Figure 80. The RF output spectrum with 8 GHz span

Chapter 6

Conclusions

A fully integrated, fast-locking fractional-N frequency synthesizer for wireless communications that offers a high integration ability, technological robustness, fast locking time, low noise level, and multi-mode flexibility has been proposed and demonstrated with a 0.18 um CMOS technology.

In the proposed frequency synthesizer, large and inaccurate passive capacitors and resistors in a loop filter has been substituted by a programmable digital Finite Impulse-Response (FIR) filter to remove the analog continuous-time loop filter whose performance is sensitive to process and temperature variations and aging. Second, the adaptive loop-gain control proportional to the frequency difference was used to make frequency locking time fast. Finally, the phase noise and spurs have been reduced by a Multi-stAge Noise SHaping (MASH) controlled Fractional Frequency Detector (FFD) that generates a digital output corresponding directly to the frequency difference.

The proposed system is composed of Fractional Frequency Detector (FFD), reference divider, amplitude detector, variable gain block, accumulator, FIR digital filter, Digital-to-Analog Converter (DAC), VCO, prescaler, and third-order MASH engine. In the system, the FFD serves as a frequency-difference gauge between the $f_{reference}$ and the $f_{feedback}$, and outputs a digital value that is directly proportional to the frequency difference. Then, the output is fed to the variable gain block, whose gain is proportionally controlled by the amplitude of the FFD output. Because of this adaptive

gain control, the acquisition time is reduced; however, the system performance after the locking is not affected by the acquisition-mode characteristics. The signal multiplied by a gain is low-pass filtered by an accumulator. Then, the filtered data is divided into two parts: the Most Significant Bit (MSB) bits part that controls the switches of the switched-current VCO and the Least Significant Bit (LSB) bits part that is followed by a FIR digital filter and a DAC. The LSB bits part controls the tuning voltage of a Voltage Controlled Resistor (VCR).

The MSBs and the LSBs then determine together the coarse and fine frequency ranges of the VCO output by controlling the switches that adjust the amount of the tail current and the tuning voltage of a VCR. After that, the output signal of the VCO, f_{out}, is divided by the prescaler because developing a FFD that operates reliably at 2.4 GHz or higher is rather difficult. Next, the divided data frequency, $f_{feedback}$, is compared with the reference frequency. Through these procedures, the frequency acquisition is completed. After the frequency locking, the phase locking is accomplished through phase acquisition by resetting the VCO.

A third order MASH engine and a FIR digital filter were used in the designed architecture to produce fractional output frequency. The FFD, which is made up of a down counter and a sampler, counts the $f_{feedback}$ clock pulse downward during the reference period. Thus, the modulus control value N is set by the initial value of the down counter. The fractional effect can be obtained by adding the output value of a third-order MASH engine and the modulus control value N. However, this change of modulus results in a rapid variation of the accumulator LSB bits part value. Thus, filtering is needed to remove high-frequency elements. The filtering function is

performed by FIR digital filter. After the filtering, the data is converted to an analog signal and used as the tuning voltage for the VCR.

The proposed frequency synthesizer's analysis, design, and simulation have been carried out at both the system and the circuit levels. Then, the performance was also verified after fabrication and packaging.

The pad-included chip area for the system is 1137 um * 1148 um and the chip consumes 19.2 mA for a 1.8 V supply voltage. The phase noise at a 2 MHz offset is –102 dBc/Hz when the center frequency is set to the 2.4 GHz. The frequency operating ranges are 2.4 GHz ~ 2.4853 GHz. The reference sideband spurs are – 48 dBc.

Because the effects of closed-in VCO phase noise can be minimized if PLL loop bandwidth and phase comparison frequency can be kept high, a fractional-N frequency synthesis technique can be utilized along with a ring oscillator VCO to produce the required local signal for the system. So, in order to reduce the VCO phase noise and the digital filter area, the wide-bandwidth, low-order loop filter has been used in the proposed system. However, the high frequency noise power occurring in the MASH and the in-band noise coming from the reference signal are not suppressed well enough due to the wide-bandwidth, low-order loop filter. Therefore, to reduce the phase-noise degradation caused by high power noise coming from the noise shaping in the MASH and the reference signal, the loop bandwidth needs to be narrower. The higher substrate noise caused by the digital circuits in the system functions as another phase-noise degradation source.

The contribution of this research is to demonstrate the possibility of a fully integrated, fast-locking fractional-N frequency synthesizer for wireless communication

applications that offers a high integration ability, technological robustness, fast locking time, low noise level, and multi-mode flexibility with a 0.18 um CMOS technology. Specifically, the frequency synthesizer does not need to use any external passive or active component because the loop filter is implemented using digital FIR filter. Therefore, the full chip has been integrated on a die and the performance of the system is not affected by the variation of the passive elements' characteristics such as inductors. The fast locking speed is acquired using the adaptive loop-gain control proportional to the frequency difference. Lastly, the locking range of the proposed frequency synthesizer is only limited by the VCO locking range and any output frequency resolution can be obtained because the division ratio is determined by the simple initial value of the FFD. So, multi-mode, multi-application system can be easily implemented with the simple, programmable digital loop filter.

To reduce phase-noise degradation and to prove the possibility of multi-mode, multi-application adaptability, the FIR digital loop filter needs to be replaced with the programmable digital filter. Then, the fully integrated frequency synthesizer whose loop filter is replaced with a programmable digital filter will be fabricated and tested in the same environment.

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